Chip Scale 3-D Topography Synthesis

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ABSTRACT

We propose a novel approach to perform the chip scale mask to topography mapping by building a library of repetitive mask patterns. We call them vicinity patterns. They describe a collection of mask features in close proximity. This pattern library is used to synthesize 3-D topography of an arbitrary part of the chip topography. We define some process-related parameters, which we call critical interaction lengths, as a basis for mask decomposition into the vicinity patterns.

Keywords: topography, 3-D lithography modeling, printability analysis, pattern matching.

1. Introduction

Traditional lithography simulation employs scalar modeling of aerial image of 2-D layout. Unfortunately, this is insufficient to synthesize realistic topography of a deep submicron IC where rigorous 3-D simulation is necessary due to very small feature sizes, large NA and small depth of focus. However, 3-D simulation has a prohibitively high cost when applied to an entire chip.

We propose (see Figure 1) to solve this problem by identifying repetitive patterns in a given mask and thus defining a set of mask patterns that have to be simulated and characterized in detail. We call them vicinity patterns since each such pattern describes several features in close proximity. The size of a pattern is determined by critical interaction distances specific for a given set of process parameters. We organize a database of vicinity patterns, with each pattern having assigned its attributes such as 3-D topography, OPC pattern, etc. These attributes may be reused whenever they are needed. Consequently, we define a mask to topography mapping (MTTM) for the entire chip as a composition of the mappings defined for all respective vicinity patterns. Topography modeling in this work is done with METROPOLE-3D [2] and includes simulation of: aerial image, photoresist exposure, post-exposure bake and development for DUV lithography.

This paper is organized as follows. Critical interaction distances and their characterization methodology are introduced in Section 2. The vicinity patterns are discussed in Section 3. Section 4 contains discussion of how the pattern database is used. Section 5 contains an example of topography synthesis based on the vicinity patterns. Section 6 presents conclusions.

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2. Critical Interaction Distances

Our approach to identification of mask features is based on the observation that the printed image in any location in IC topography depends only on the configuration of mask edges in close proximity. Moreover, as was also noticed in [4], in the case of masks defined by polygons, the only mask regions which require 3-D consideration for topography simulation are the ones in vicinity of vertices of mask polygons. In addition, if a given region of interest is located far enough from all vertices it can be characterized by 2-D simulation. In general, shapes which belong to more than one mask may affect topography in a given region (for example, region of poly layer near the MOS transistor). In such a case, the points of intersection of shape borders from the respective masks are treated as additional mask vertices (intersection of poly and active masks for example).

Consequently, we assume that the interaction of edge segments and vertices can be ignored if these entities are separated by more than a certain critical distance. We define three kinds of such critical interaction distances (CID's) (Fig. 2):

- $\mathbf{L}_{cr}$ - distance measured along the border of a mask polygon. We assume that if two subsequent vertices are separated by more than $\mathbf{L}_{cr}$ from each other, their influence on topography profile may be considered separately.
- $\mathbf{L}_{in}$ - distance measured from a given vertex in the direction of interior of the shape this vertex belongs to. We assume that if two vertices are separated by more than $\mathbf{L}_{in}$ from each other, then their influence on topography profile may be considered separately.
- $\mathbf{L}_{ex}$ - distance measured from a given vertex in the direction of exterior of the shape this vertex belongs to. We assume that if two vertices are separated by more than $\mathbf{L}_{ex}$ from each other, then their influence on topography profile may be considered separately.

We treat the CID's as characteristic parameters of a given manufacturing process and equipment set. In order to estimate the values of CID's heuristically, we run a number of topography simulations for a set of test patterns containing the interacting mask features separated by different distances. Then, we compare the results against the ones obtained for the corresponding isolated features. An example of such a procedure for one test pattern is shown in Fig. 3. The mask feature which we focus on in this simulation is contained inside the region of interest marked on the figure. In the case we were investigating, we run such simulations for 18 different parametrized test patterns and picked the respective worst case distances as values of $\mathbf{L}_{cr}$, $\mathbf{L}_{in}$, $\mathbf{L}_{ex}$. The same patterns can be manufactured and measured to obtain more thorough characterization and to tune the topography simulator.

3. Vicinity Patterns

The critical distances determine the sizes of what we call “vicinity patterns”. In order to define them, we will first introduce the following auxiliary concepts: soft edge, subchain of vertices and the subchain shadow. The discussion below is presented in context of contours - simple polygons which represent the borders of possibly multi-connected mask polygons. A contour has an attribute of orientation so that it can describe either a solid or a hollow. This canonical representation of masks is described in [1] where we have proposed an isometry invariant pattern matching algorithm for mask contours.

Given a single edge segment of a contour which is longer than 2*$\mathbf{L}_{cr}$, by the **soft edge** we understand a portion of this edge which is obtained by subtracting a section of length $\mathbf{L}_{cr}$ from each side of this edge segment. Note that the concept of soft edge allows for treatment of long enough edges of different lengths in the same way. Qualitatively speaking, if we disregard non-planarity issues, a soft edge corresponds to a place which “is a candidate” for a 2-D analysis if all contour vertices are “far enough”.

By **subchain** we understand a specially marked part of a soft edge or such a sequence of edges of a contour, for which each two subsequent vertices created by neighboring edges are distant by no more than $\mathbf{L}_{cr}$. If the sub-chain includes all the edge segments of the contour, then it is called the **closed sub-chain**. If the sub-chain begins and ends at the soft edge, it is called the **proper sub-chain**. Two sub-chains of a contour which share at least one vertex are called the **overlapping sub-chains**. By the edge segment belonging to the sub-chain we will understand each edge which connects vertices of the subchain or such part of the first or last edge in the subchain which is not longer than $\mathbf{L}_{cr}$. These concepts are illustrated in Figure 4. The “specially marked part of a soft edge”, mentioned at the beginning of this paragraph, is a part which requires 3-D analysis due to proximity of some vertices (see example in Section 5 below).

By the **subchain shadow** (Figure 2) we understand a region created as a “halo” around a given chain of vertices of a mask contour in such a way that it extends by:

- $\mathbf{L}_{ex}$ from each vertex of the subchain in the direction of the contour exterior,
- $\mathbf{L}_{in}$ from each vertex of the subchain in the direction of the contour interior,
- $\mathbf{L}_{ex}$ in the normal external direction from each edge of the subchain,
- $\mathbf{L}_{in}$ in the normal internal direction from each edge of the subchain.

For a given subchain, the shadow marks a region of interaction of vertices belonging to this subchain and neighboring mask features. In other words, we use subchains as “alignment marks” for clipping out mask fragments in search for repetitive patterns and the shadow is our clipping region. As illustrated in Figure 5, these clips are our vicinity patterns. More precisely:

A **vicinity pattern** is a configuration of mask vertices and edge segments within a subchain shadow. The vicinity patterns are defined in such a way that we can apply a signature-based pattern matching technique to locate them easily within the layout even if the subsequent instances of vicinity patterns are rotated by a multiple of $\pi/2$, or mirrored. The matching technique, which we developed for this purpose, is beyond the scope of this paper and will be published separately.

An important question to ask at this juncture is: how many vicinity patterns are needed to analyze a mask of a microprocessor? At the time of this writing, we cannot provide the exact answer to this question yet. However, we have processed a number of relatively large layouts (up to the size of 50 000 transistors) of parts of a microprocessor and other digital circuits, and we obtained encouraging results, suggesting that the number of patterns is manageable (see Figure 6). Although there is a significant number of patterns that repeat only once, the majority of them are repeated tens or hundreds of times. We also noticed in our experiments, that accounting for rotations and reflections of patterns significantly reduces their number.

4. Pattern Library

As shown in Figure 11, we organize the topography database around patterns and pattern instances. We keep the vicinity patterns and their repetitive attributes (such as 3-D topography) in a pattern database and can reuse the results of topography simulation any time a given vicinity pattern is found in layout. Reuse of topography simulation results is analogous to using cells from a library and cell instances in IC design, and is similar to the idea proposed in [1] for the database of repetitive contours. Such an approach allows for a significant reduction of data volume in 3-D representation of large IC topography. Moreover, the 3-D data can be generated on the fly (instantiated) when it is needed. This is possible because we can quickly generate a unique signature for a given vicinity pattern having any of the pattern instances (as, for example, the one shown in Fig. 5). The signature allows us to query the pattern database very efficiently to obtain the pattern attributes. If the attributes are not available (because, for example, the pattern is not in the database yet) they are generated first time they are needed and then can be reused. Note that the pattern database may be required to store a very large volume of data, but the data can be organized in a way compatible with very efficient commercial database servers.

5. Example

To illustrate the idea of 3-D topography synthesis, we show below an example of mask to topography transfer for a part of an IC layout printed in DUV lithography (λ=248nm, NA=0.55, σ =0.8, defocus=0.0). For illustration purposes, we set $L_{cr}=L_{in}=L_{ex}=0.9$ μm which is a value larger than

the value of 0.6μm estimated for this process. We have chosen the mask pattern complexity (Figure 8) in such a way that it is easy to illustrate all the aspects of the process. First, we identify all the instances of subchains which are incident with our region of interest. This is shown in Figure 9, where each such subchain has been assigned a unique number. This number is used in later figures to mark where a given pattern is coming from. Note that some parts of the soft edges are marked as separate subchains (numbers 6, 7, 14, 15 and 20-29) since they have at least one vertex in their vicinity. Fig. 10 shows all kinds of subchains incident with our region of interest. For each vicinity pattern, we perform 3-D topography simulation in a way shown in Figures 11 and 12. First, we extend the simulation region ("padding region" in Figure 11) to assure that the result in the vicinity of the subchain is not disturbed by the boundary conditions not matching the real layout. For a given pattern, the only interesting part of simulation result in our case is the one in the proximity of the pattern subchain as marked on the photoresist profile in Figure 12. However, in some other cases (printability analysis, for example) larger portion of the pattern topography profile may be interesting. Fig. 13 shows all vicinity pattern instances found within our region of interest. It has to be noted that there are only 12 different patterns. Moreover, what is not shown in the figure, we also have to perform simulations for a 2-D case of three parallel lines. The pattern number 6 illustrates a common case when the patterns are not repeated (the "tail" of the frequency plot in Figure 6): a small part of a layout feature is contained in the subchain shadow.

Figure 14 illustrates how the topography synthesis is actually performed: there is a number of 2-D and 3-D regions to be stitched. For each subchain we identify its vicinity pattern and the 3-D topography implied by it. In the remaining regions, we insert the topography profile resulting from 2-D modeling.

6. Conclusions

In this paper we have presented a decomposition method which divides a mask layout into small, repeatable parts called the vicinity patterns. The result of this decomposition may be used for synthesis of arbitrarily large portions of 3-D chip topography by reuse of topography attributed to the patterns. The decomposition into patterns is done with regard to critical interaction ranges characteristic to a given manufacturing process. This is a more systematic way to decompose large layout for 3-D simulation than decomposition by hand commonly used with today's lithography simulators.

Once the vicinity patterns for a given mask are found, they can be used for printability analysis. Moreover, each vicinity pattern can have many topography profiles for different values of process parameters (such as photoresist thickness, depth of focus etc.) assuming that the values of CID's remain the same. The vicinity patterns are also very useful for localization of these features on the

mask which are not going to print well after shrink. Due to space limitation we have not discussed the OPC or PSM issues. It has to be stressed that in our methodology, the vicinity patterns are defined in terms of design masks. The OPC-related modifications of mask shapes and the phase shifting regions may be introduced after the patterns are defined. In the case of OPC, this is the way to deal with the "data volume explosion" problem and allows to minimize the processing time while accounting for 3-D effects. It is also compatible with the practical approach to OPC proposed in [5]. Moreover, since we use rigorous 3-D lithography simulation, we can, in a natural way, account for multilayer, non-planar patterns such as the ones of a gate layer in the vicinity of a MOS transistor.

Our future work will include experiments with test structures for estimation of critical interaction lengths, more investigations of multilayer patterns, and automated printability analysis for OPC and shrink.

7. Acknowledgments

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8. References

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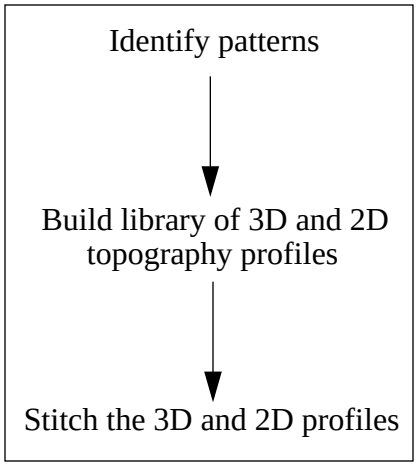

Figure 1. The approach to topography simulation presented in this work.

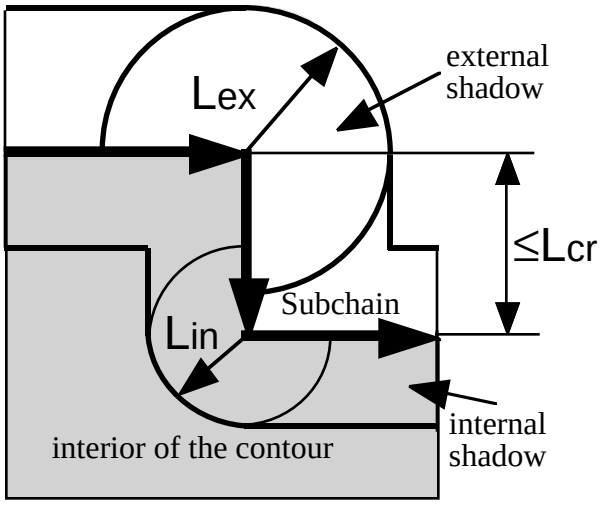

Figure 2. Critical interaction lengths and the subchain shadow.

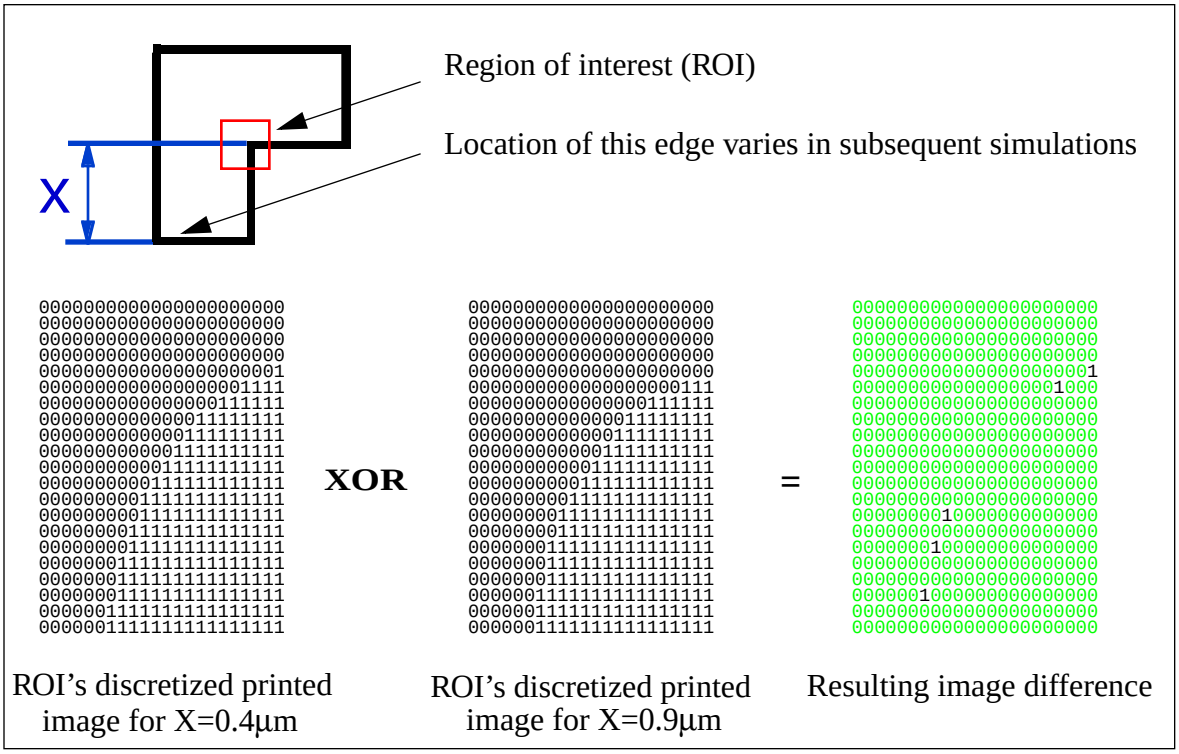

Figure 3. An example of experiment to estimate a value of critical interaction lengths. The results are discretized on a 20nm grid.

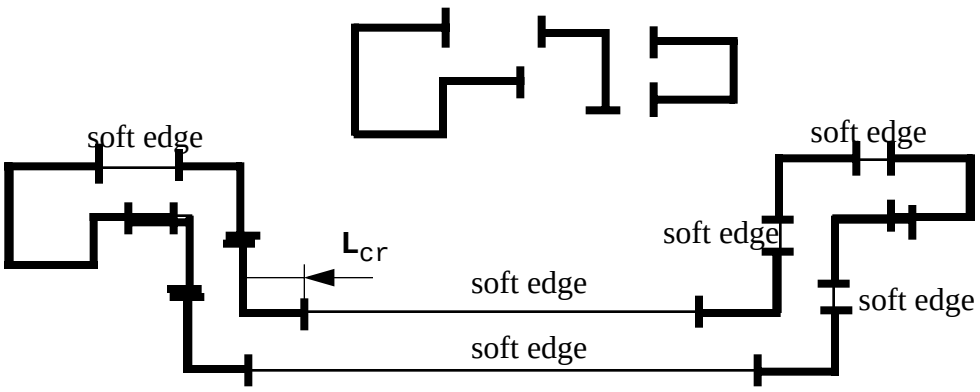

Figure 4. Subchains and soft edges for a mask polygon example.

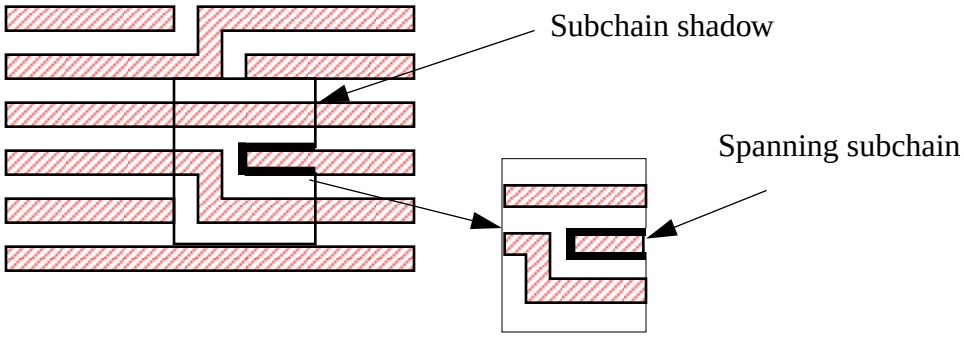

Figure 5. Formation of a vicinity pattern based on a shadow of a given subchain.

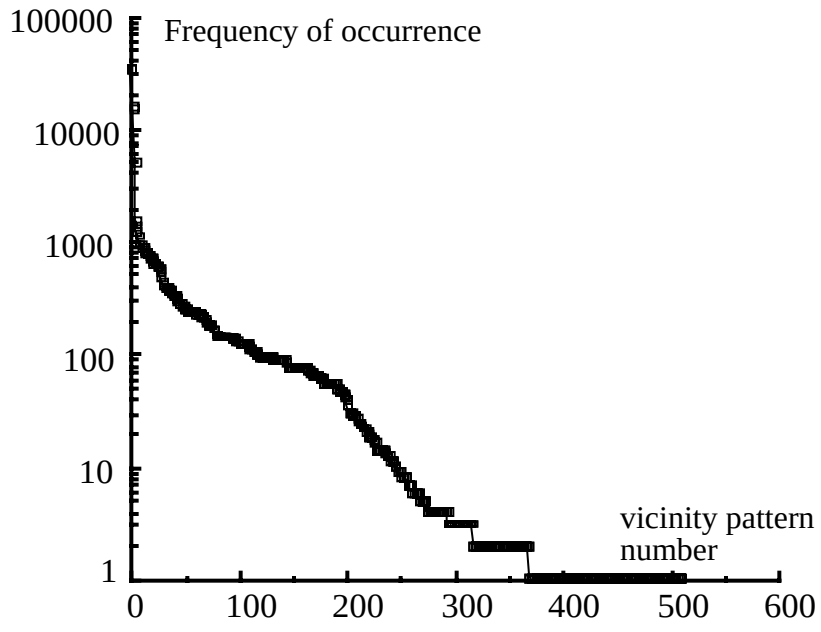

Figure 6. Frequency of repetition of vicinity patterns in a design example. A fragment of a poly mask for a random logic circuit (standard cell design style, approx. 15000 transistors, shadows of soft edges were omitted in this example).
Line width = Line spacing = 0.3 μm; $L_{cr} = L_{in} = L_{ex} = 0.6\mu m$

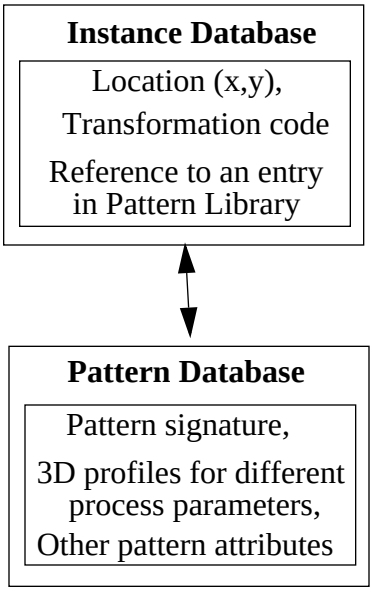

Figure 7. Pattern-based organization of 3-D topography database.

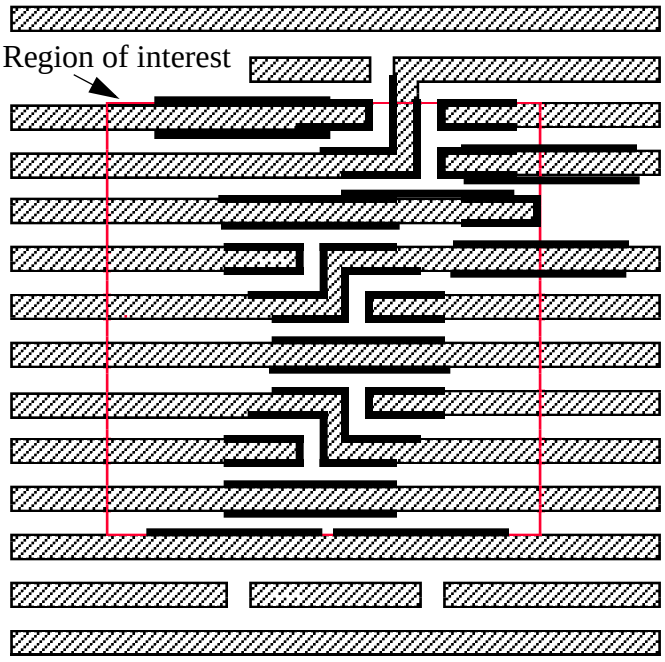

Figure 8. Example of mask region for topography modeling. All line widths and spacings in the layout are 0.3µm. Thick lines mark subchains.

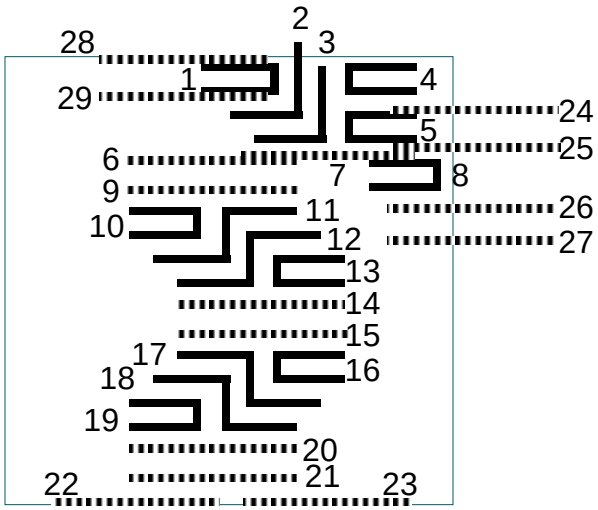

Figure 9. Subchains incident with the region of interest. 3-D fragments of soft edges are drawn with a dashed line.

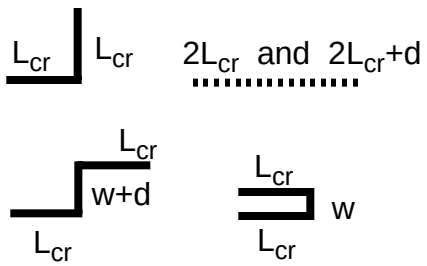

Figure 10. Subchains defined in our example. Dimensions: Lcr=0.9 µm, w=0.3µm, d=0.3µm

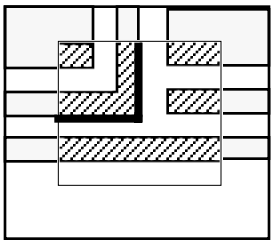

Figure 11. Each vicinity pattern is extended with padding regions for the purpose of simulation or measurement.

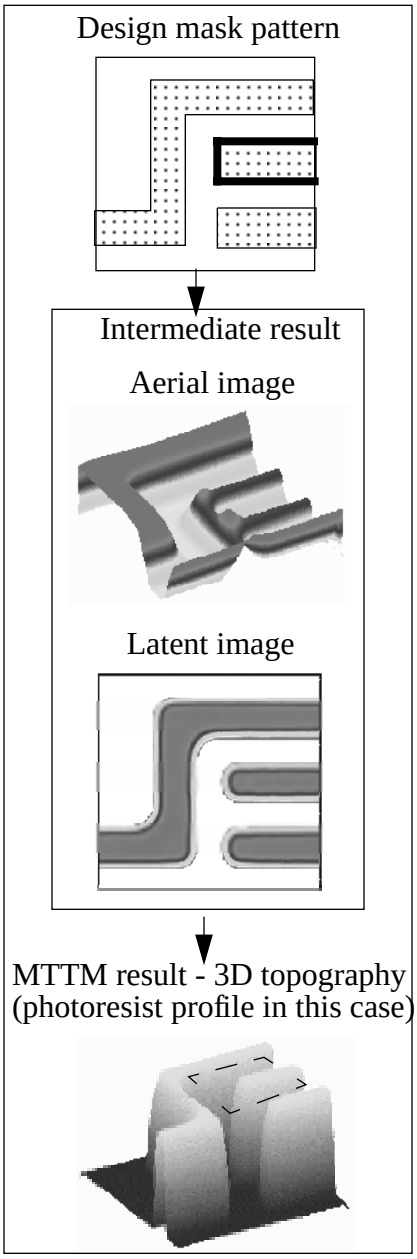

Figure 12. Mask to topography mapping for a vicinity pattern example.

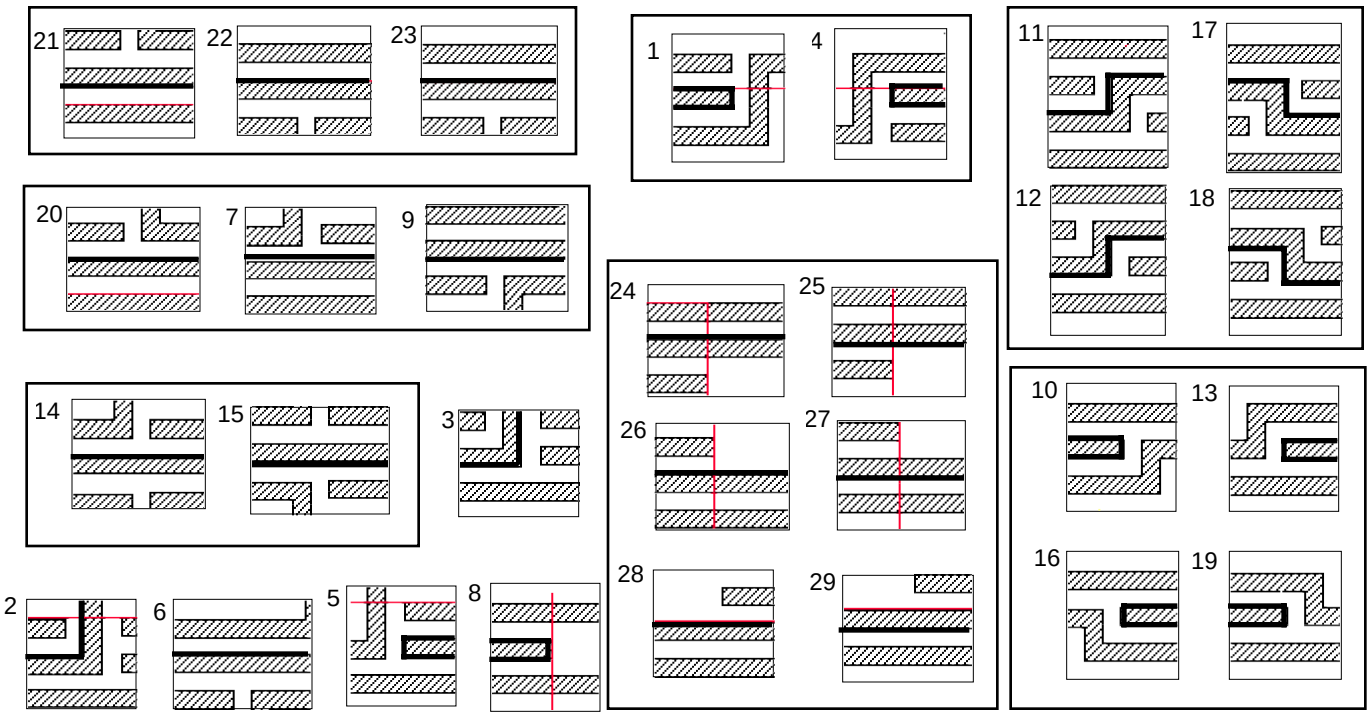

Figure 13. 12 different 3-D vicinity patterns were found in the example from Fig. 9.

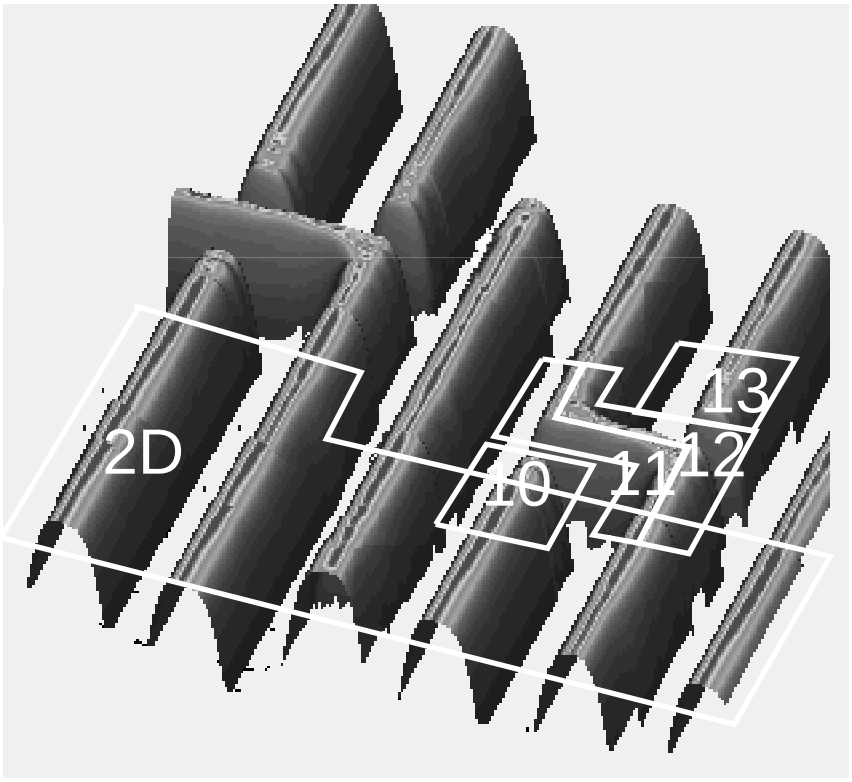

Figure 14. Illustration of 3-D and 2-D topography profiles stitching.