Design Compliant Source Mask Optimization (SMO)

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ABSTRACT

Source Mask Optimization (SMO) is required to extend the use of 193 water immersion lithography to the 22nm technology node. Although SMO is being aggressively pushed in volume production the layout design implications of this technology have not been openly discussed. In this paper, the impact of layout design style on simultaneous SMO of Logic and SRAM is studied. In particular the improvements in pattern control offered by the pdBRIX template-based design methodology and its compliance with ASML's Tachycon SMO and Flexray source will be highlighted. We evaluate the common process window (PW) for SRAM and for pdBRIX templates and compare it to the common process window for SRAM and "gridded" logic designs. The PW of both logic design styles is first calculated by performing SMO for the SRAM only and mask optimization for the logic using the SRAM optimized source. This result is compared to PW for the logic blocks by performing simultaneous SMO for the SRAM and logic designs. In each case Tachyon SMO was used to simultaneously optimize the FlexRay source and the binary mask for the Contact, Metal 1, Via 1 and Metal 2 layers.

In Figure 1 below, the PW is shown for one of the experiments. The overlapping PW in Figure 1a from SMO on the SRAM only has a 120nm DOF at 5% EL. If one performs simultaneous SMO over the SRAM and pdBRIX templates, the overlapping PW of the SRAM in Figure 1b also observed to be 120nm DOF at 5% EL. This shows that the patterns chosen in the pdBRIX templates do not increase the design complexity. In other words the PW is limited by the SRAM design.

Next, in figure 2, a comparison of the PW for the pdBRIX templates is shown. In Figure 2a, the mask for the pdBRIX templates block is optimized using the source in Figure 1a from SMO on the SRAM only. Here we experience a 95nm DOF at 5% EL. In Figure 2b, the source and mask was simultaneously optimized for the SRAM and pdBRIX templates. By doing so the PW is increased to a 120nm DOF at 5% EL. In summary, we have shown that there is an advantage of optimizing the SRAM and logic together rather than optimizing the SRAM only. This result motivates the need for SMO across different components on a chip to maximize PW.

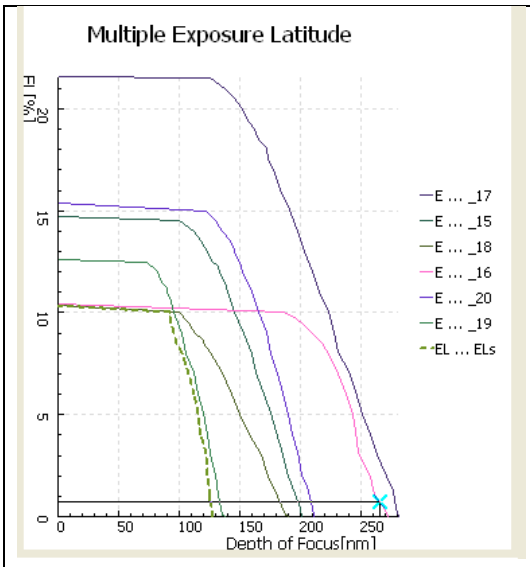

Figure 1a. Metal 1 PW at multiple cutlines in the SRAM for source mask optimization on the SRAM cell. The overlapping PW is the dotted green line.

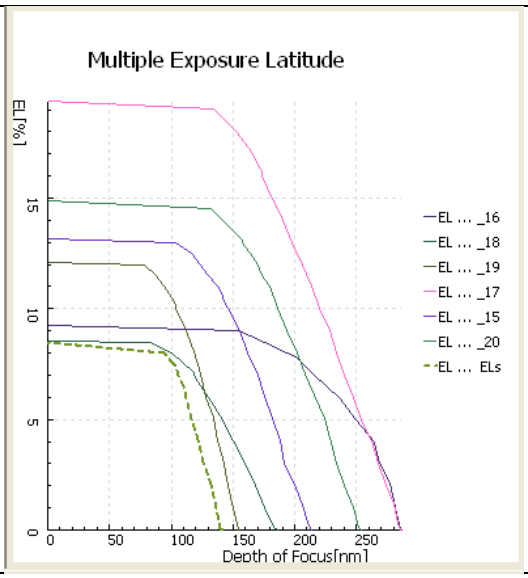

Figure 1b. Metal 1 PW at multiple cutlines in the SRAM for simultaneous source mask optimization on the PDF logic bricks and the SRAM cell. The overlapping PW is the dotted green line.

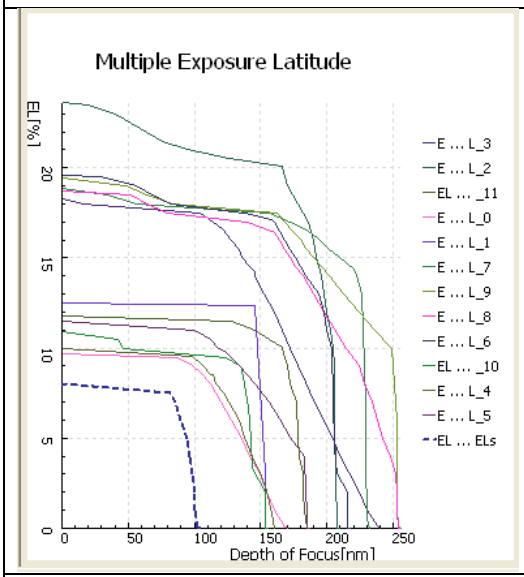

Figure 2a. Metal 1 PW at multiple cutlines in the SRAM and logic for mask optimization on the logic blocks using the SMO source from the SRAM in Figure 1a. The overlapping PW is the dotted blue line.

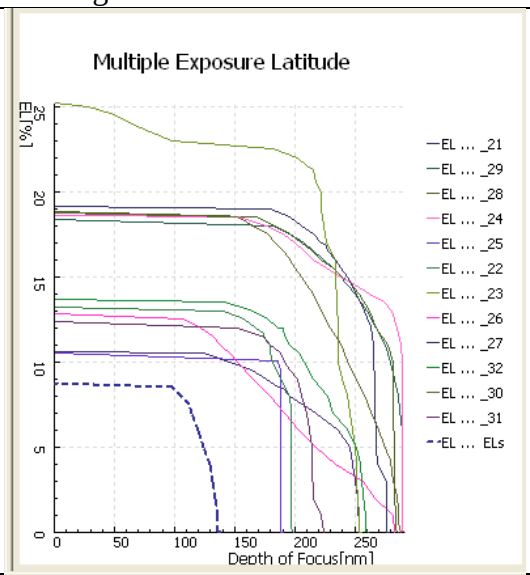

Figure 2b. Metal 1 PW at multiple cutlines in the SRAM and logic for simultaneous source mask optimization on the logic blocks and SRAM. The overlapping PW is the dotted blue line.