Holistic Yield Improvement Methodology

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ABSTRACT

As new products and processes are being introduced into IC manufacturing at an accelerated rate, yield learning and ramping are becoming more challenging due to the increased interaction between the design and process. Compared to random defect caused yield losses, systematic yield loss mechanisms are becoming more important, thus initial yield ramping process becomes more challenging. A “holistic” yield improvement methodology has been proposed and implemented to significantly reduce the yield ramp time and maximize the profit for the semiconductor manufacturer. This new approach to yield improvement bridges the gap between design and manufacturing by integrating process recipe and design information with in-line manufacturing data to gain an enhanced understanding and subsequent determination of the process and design architecture issues that affect yield and performance. With this methodology yield is improved not just by eliminating defects, but also by resolving parametric and systematic problems. The result is higher yield and performance in a fraction of time required by traditional “defect-based” methods.

I. INTRODUCTION

The challenges and rewards of designing and manufacturing leading edge integrated circuits have scaled with the complexities of chip functionality. This increase in IC functionality has been made possible by a continuous drive towards smaller feature sizes. Due to the decreasing dimensions of semiconductor structures, the manufacturing sensitivity to critical design and processing parameters has risen dramatically. Vertical integration techniques and multi-level interconnects, which are becoming more common in modern technologies, have driven up the number of critical processing steps to several hundred [1]. These trends are expected to continue for the next decade. In addition, the increase in IC functionality has come with skyrocketing capital spending, e.g., $2-10bn [2] for a fabrication facility. Given this high level of investment, it is critical for IC manufacturers to increase manufacturing efficiency and reduce manufacturing costs to obtain a better return on their investment. Another important

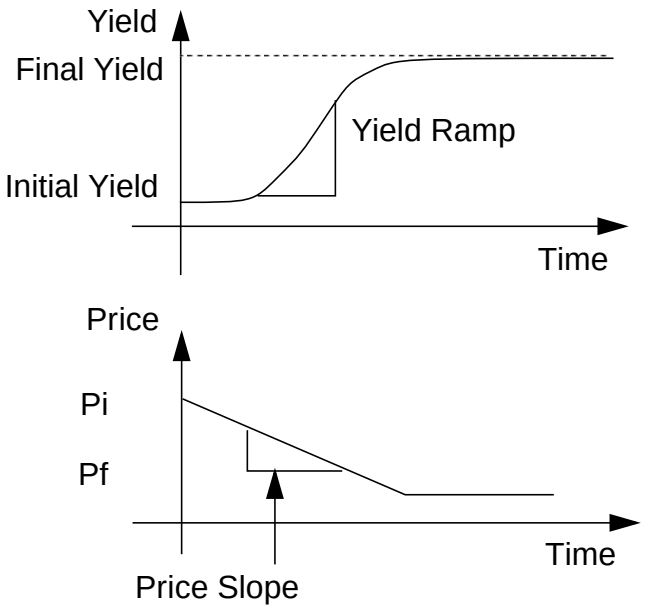

Figure 1. Yield and price curves of a typical product.

consequence of rapid increasing IC functionality is the shortened product life. Driven by trends, such as system-on-chip, new products and processes are being introduced into IC manufacturing at an accelerated rate to satisfy narrowing market windows.

In this age of multi-billion dollar semiconductor fabrication facilities and increased time-to-market pressures, rapid yield learning is essential to achieve profitable production of integrated circuits. To be competitive, the cost per die must be minimized while quickly ramping the manufacturing yield to an economically acceptable level. Increasing the initial yield and rate of the yield ramp are the biggest drivers of product profitability making final product yield (Y_F) significantly less important than in the past. As shown in Fig. 1, the price of a product usually gradually decreases after it reaches the market place. If a semiconductor manufacturer is able to increase the slope of the ramp rate, much more products can reach the market while the price is still high. In other words, the yield ramp rate of a product is more important to the profit margin than the high volume production yield.

In high volume production, random defects caused by particulate contamination are typically the dominant reason for yield losses. Contamination defects which result in possible yield loss can be

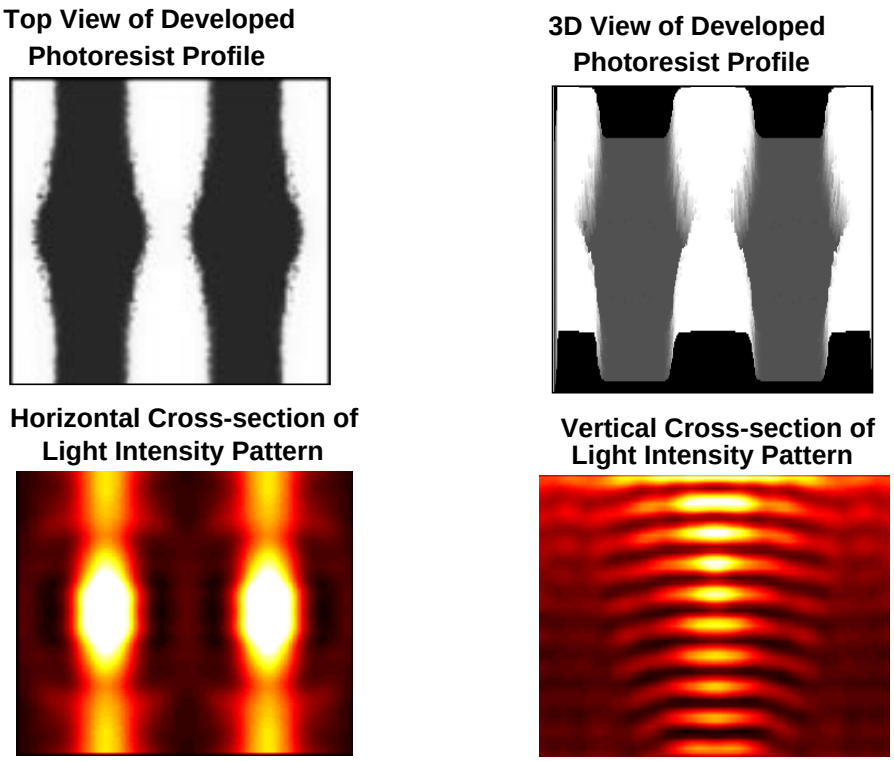

Figure 2. Simulation results of metal line structure, reflective notching is observed.

introduced at any one of hundreds of the process steps. The size of these defects which cause yield loss may be smaller than the design rule and the sensitivity limit of metrology equipment. This fact poses a challenge to modern deep submicron VLSI manufacturing technologies: how to accurately evaluate the yield impact of these particles. It has been seen that defects may propagate and grow throughout the process flow, and as a result cause faults in the final product. In recent studies, it was found that there are two major defect propagation mechanisms, namely inter-layer and intra-layer defect propagations[3].

In addition, yield learning is becoming more difficult due to the increased complexity of the products, the processes, and their often subtle interactions. Various new emerging process technologies have induced new problems, especially during the yield ramping process. For example, the critical dimension (CD) of the active device is fast approaching the wavelength used in photolithography process. This has introduced printability problems such as Lpoly variation and reflective notching effect. While within chip variation is typically due to effects such as micro-loading in the etch, variations in photo resist thickness,

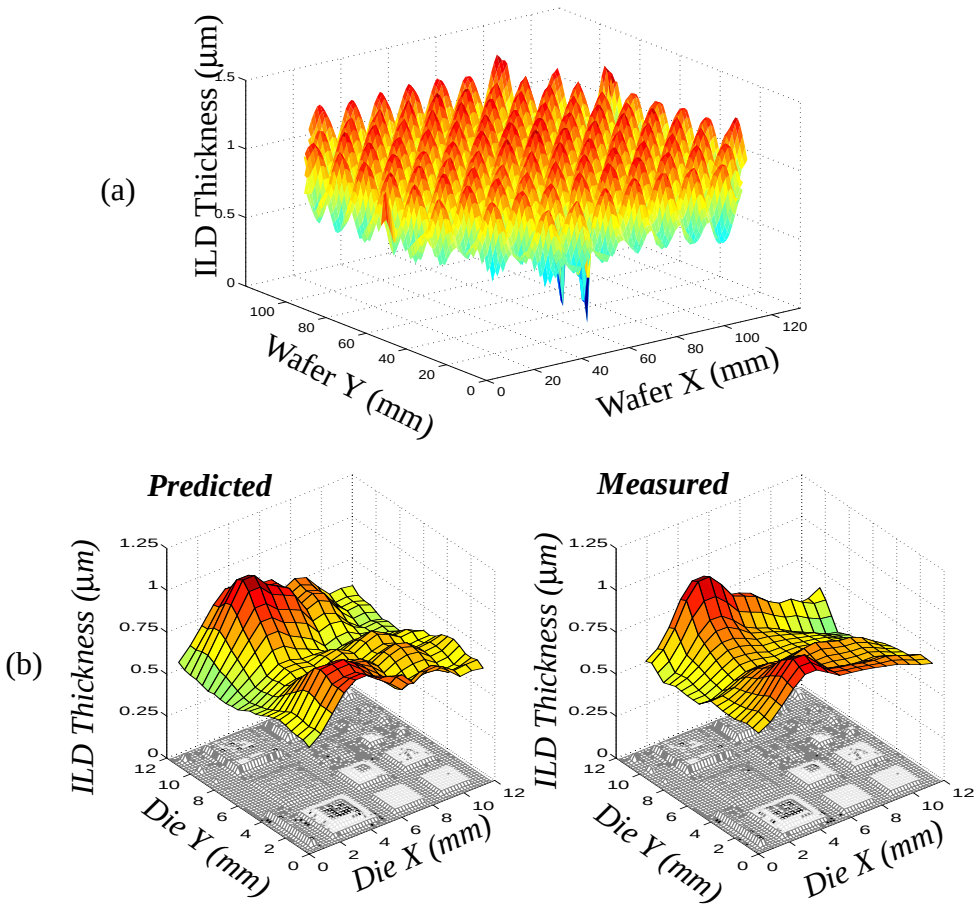

Figure 3. Dielectric thickness variations: (a) intra-wafer ILD variation; (b) intra-die ILD variation.

optical proximity effects, and stepper within field aberrations, the reflective notching is caused by the optical interaction between exposing light, resist and substrate structures. Fig. 2 shows the simulation result of a reflective notching effect caused by the reflective substrate[5].

CMP is used to planarize the dielectric. The amount of material removed is highly dependent on the pattern density of the underlying layer [4]. As a result, the dielectric thickness variation within a chip can be thousands of angstroms. Typically, the within chip variation is larger than the within wafer variation. Like the poly critical dimension variation, most of the within chip variation in not purely random but depends on the layout, CMP pad material, slurry chemistry, rotation rate, and down force applied. Fig. 3 shows an example of intra-wafer and intra-die ILD thickness variation.

As the device size shrinks below quarter micron range, the device characteristics become a more

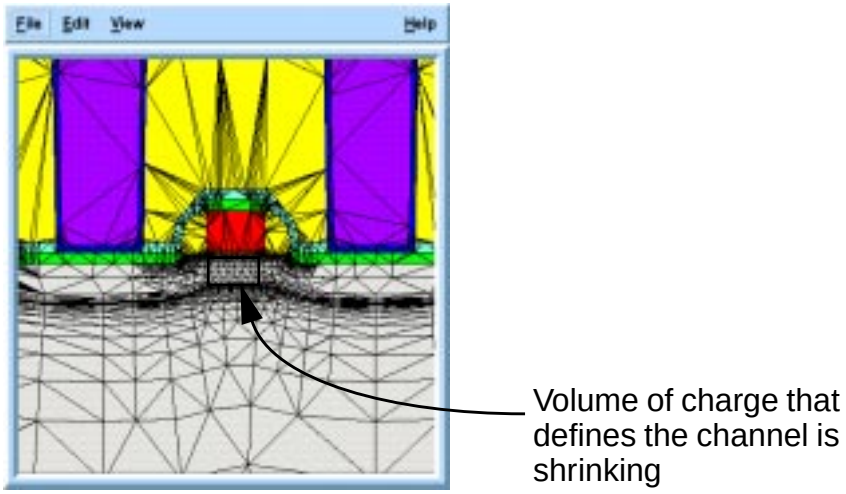

Figure 4. Channel doping variations.

important yield and circuit performance issue. Statistical fluctuations of the dopant concentration are an increasingly significant source of active device variability. With decreasing device dimensions, the number of dopant atoms in the active volume is dropping into a range where the variability due to sample size is becoming substantial. For example, consider a MOSFET with the effective channel length of 0.1 microns. The electrically active volume can be estimated to approximately: Leff*W*Dch (Dch is the thickness of the inversion layer, for modern devices approximately 0.01μm). With estimated values for Leff, W, Dch and Nch (channel doping) the active volume contains about 500 dopant atoms. The actual number of atoms is subject to statistical fluctuation is on the order of $1/\sqrt{SampleSize}$. Therefore, the statistical fluctuations of the threshold voltage and the drain current are on the order of 4% (see Fig. 4). This variability is in the range of gate length variability (Poly CD variation), which is typically as large as 10% [6].

We believe that the requirements for yield and performance ramping are changing as new technologies are introduced and the yield ramp becomes the key driver of profitability. These changes require a re-defining of the interfaces between design, test and manufacturing. In this paper, we will present a a comprehensive view of the yield problem and a “holistic” yield ramping methodology. After a discussion of our view on yield loss mechanisms in Section II, we present a hypothesis-driven holistic

yield improvement methodology in Section III, followed by a summary in Section IV.

II. Holistic View of the Modern Yield Loss Mechanisms

Yield loss mechanisms in an IC can be classified into two types: global and local disturbances [9]. Global disturbances are those that affect all the ICs on a chip or even a wafer at the same time, including random variations in either equipment settings or design variables. Examples of such disturbances include variations in temperature, resist thickness, etchant concentrations, etc. These variations can occur both within a die and across the wafer resulting in yield loss or a shift away from the nominal performance for each manufactured IC. Global variations usually affect the performance of ICs causing some ICs to miss design specifications. When the fabrication process is newly defined and is being tuned to achieve the necessary process and device parameters, the yield loss is typically due mainly to global disturbances

In contrast to global disturbances, local disturbances introduce a deformation of a small local area of an IC die. These deformations are usually referred to as random defects [10]. Random defects forming at a certain location on IC could cause the topography of the circuit to change. Local disturbances which lead to random defects arise mainly from some contamination affecting the wafer during fabrication process. When the process matures and high volume production starts, random defects are the dominant cause for yield losses.

During high volume production, defect problems are typically addressed by optically inspecting wafer surfaces during production. Making a connection between an observed defect and an electrical fault is not automated. Early in the production life cycle, design/manufacturing interplay and defect problems are addressed by manipulating design rules, resizing transistors, and using more conservative cells. An example of the yield breakdown during the yield ramping and high-volume production is shown in Table 1.

Table 1. Components of yield loss

Probe Yield Problem	Contributors to Final Yield	Contributors to Yield during ramping
Contamination	60%	48%
Design margin / Design - manufacturing interplay	14%	32%
Process variation	12%	10%
Photolith errors	10%	7%
Materials	4%	3%
Total	100%	100%

Yield improvement in the fab often refers just to the reduction in contamination caused yield loss. However, the most important factor is the final package yield which also includes parametric (e.g., speed loss, high power consumption) and functional yield loss mechanisms. Parametric and functional yield loss mechanisms can both be due to random and systematic causes (see Fig. 5). Identifying and eliminating systematic yield loss mechanisms is a key to improving the yield ramp rate and increased profitability.

As it is shown in Fig. 6, many issues which affect yield reside at the boundaries between traditional engineering groups. For example, there exists an organizational barrier between design and manufacturing groups; it is very difficult to quantify the balance between performance and manufacturing yield; trade off between cost of test vs. information content is not well understood; it is difficult to know which in-line results affect performance and yield most. These traditional barriers slow the rate at which manufacturers can ramp yield. Thus, only by taking a holistic view of yield, can the yield ramp time be minimized.

III. Holistic Yield Ramp Methodology

In this section, we present a novel yield and performance ramping methodology which is based upon a holistic view of yield. By leveraging simulation and hypothesis-driven statistical analysis, typical obstacles between traditional engineering groups are bridged. We use a combination of yield and performance prediction as well as statistically-based data analysis to isolate where the actual yield and

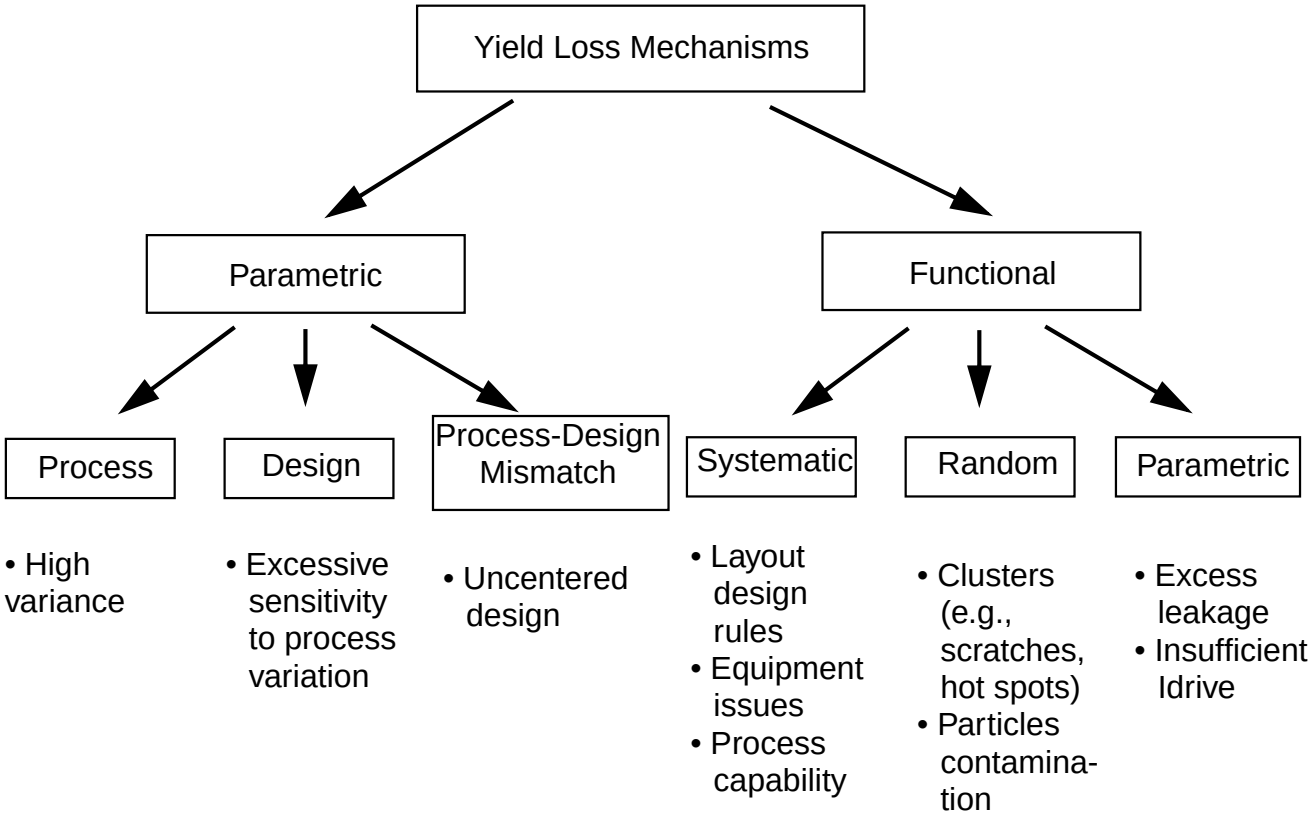

Figure 5. Yield loss mechanisms.

predicted yields are inconsistent. This situation indicates that a systematic yield loss mechanism may be present. After the yield loss mechanism is isolated, solutions are rapidly proposed and evaluated via simulation until an optimal engineering solution is found to maximize yield while achieving performance targets.

We also incorporate a hypothesis-driven work style to maintain alignment between analyses and the decision making process. Our methodology combines data from design, manufacturing, test, and the process recipe as early as possible. Simulation enables multiple solutions for each problem to be examined concurrently in a timely manner, reducing the time and expense of relying solely on lot split experiments.

The five components of the analysis streams are as follows: defect monitoring, design analysis, data analysis, process/device parametric analysis and layout/circuit parametric analysis. The design and

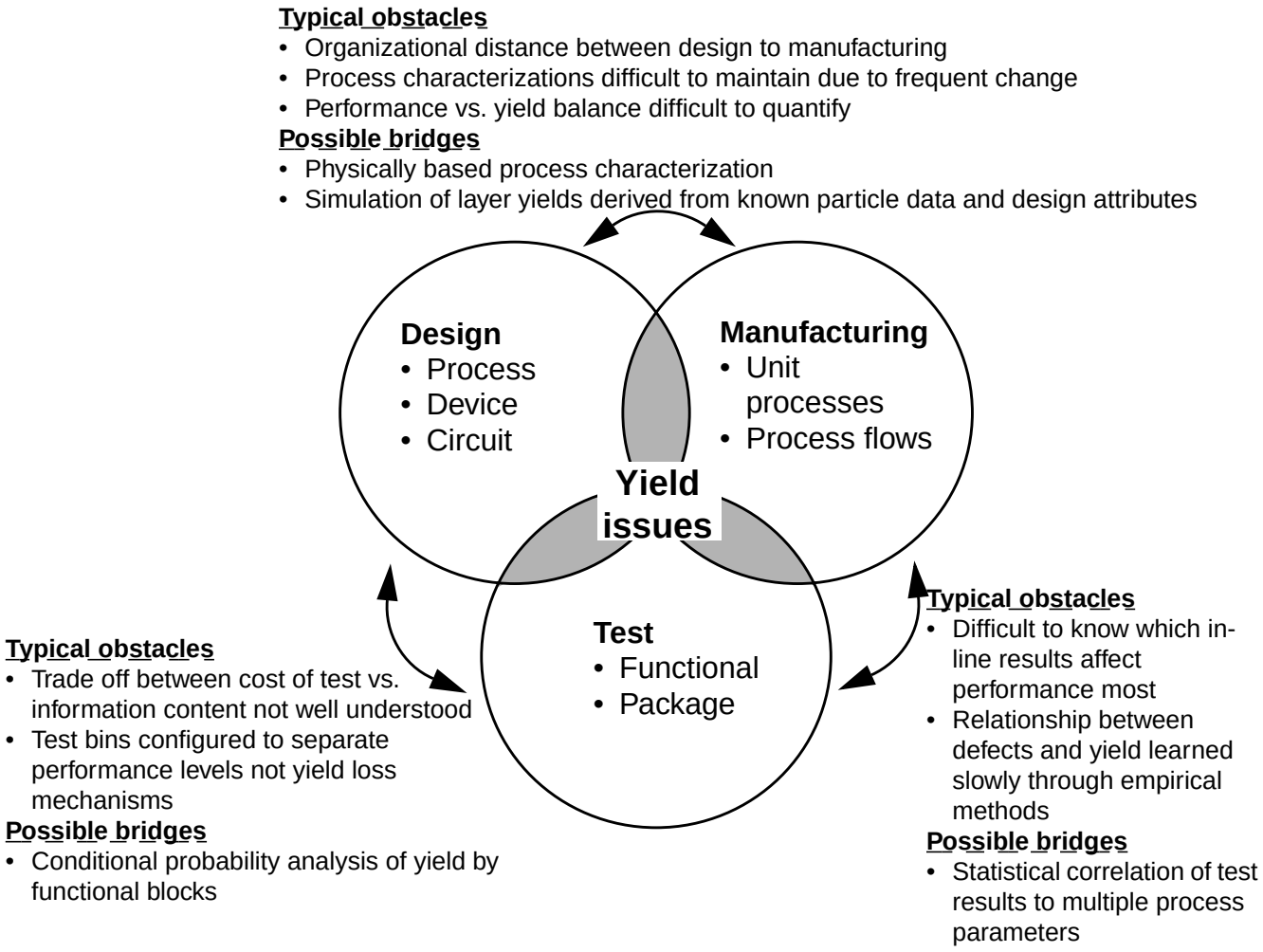

Figure 6. Holistic view of the yield.

process/device analyses support the yield prediction while the data analysis isolates the exact signatures of the yield loss mechanisms which affect the product.

Predictive yield modeling is an indispensable capability during the yield ramp phase. This is especially true when multiple yield loss mechanisms may be present including such diverse failure mechanisms as random defects, pattern-dependent effects, within-die process variation and parametric process mis-centering. To help disaggregate the effects of individual root causes on final product yield, we have developed a methodology in which limited-yield prediction is used to provide microscopic observability of physical failure mechanisms. Furthermore, application of this methodology during technology or product development allows designers to anticipate certain types of yield loss and employ

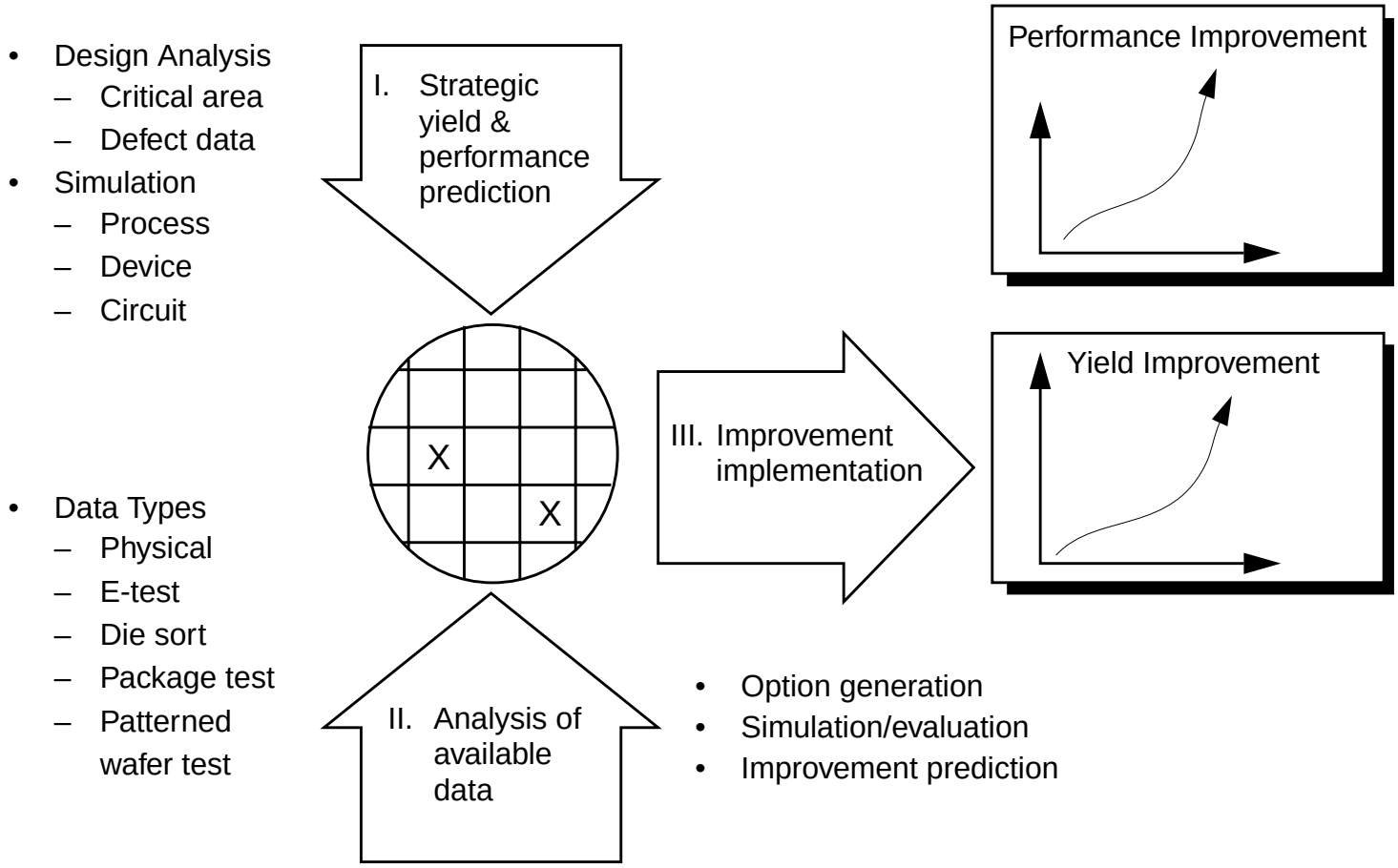

Figure 7. Overview of holistic yield improvement methodology.

appropriate design optimizations.

We focus on prediction of product- and process-specific “failure signatures” resulting from random defects. A software framework (Fig. 9) has been created to implement this methodology. Three components are used: a design analyzer (pdex), a measured data modeler (defect detective - dfd) and a defect limited-yield modeler and analyzer (lyma). In accordance with the wide applicability of limited-yield prediction, it should be noted that both the methodology and software framework presented herein have also been designed to aid with other types of yield loss analysis, including pattern-dependent, within-die process variations and parametric process mis-centering.

Both reconfigurable memory devices and advanced logic devices with embedded memory are within the scope of the methodology presented here. Detailed analysis of block, row, column, bit and other

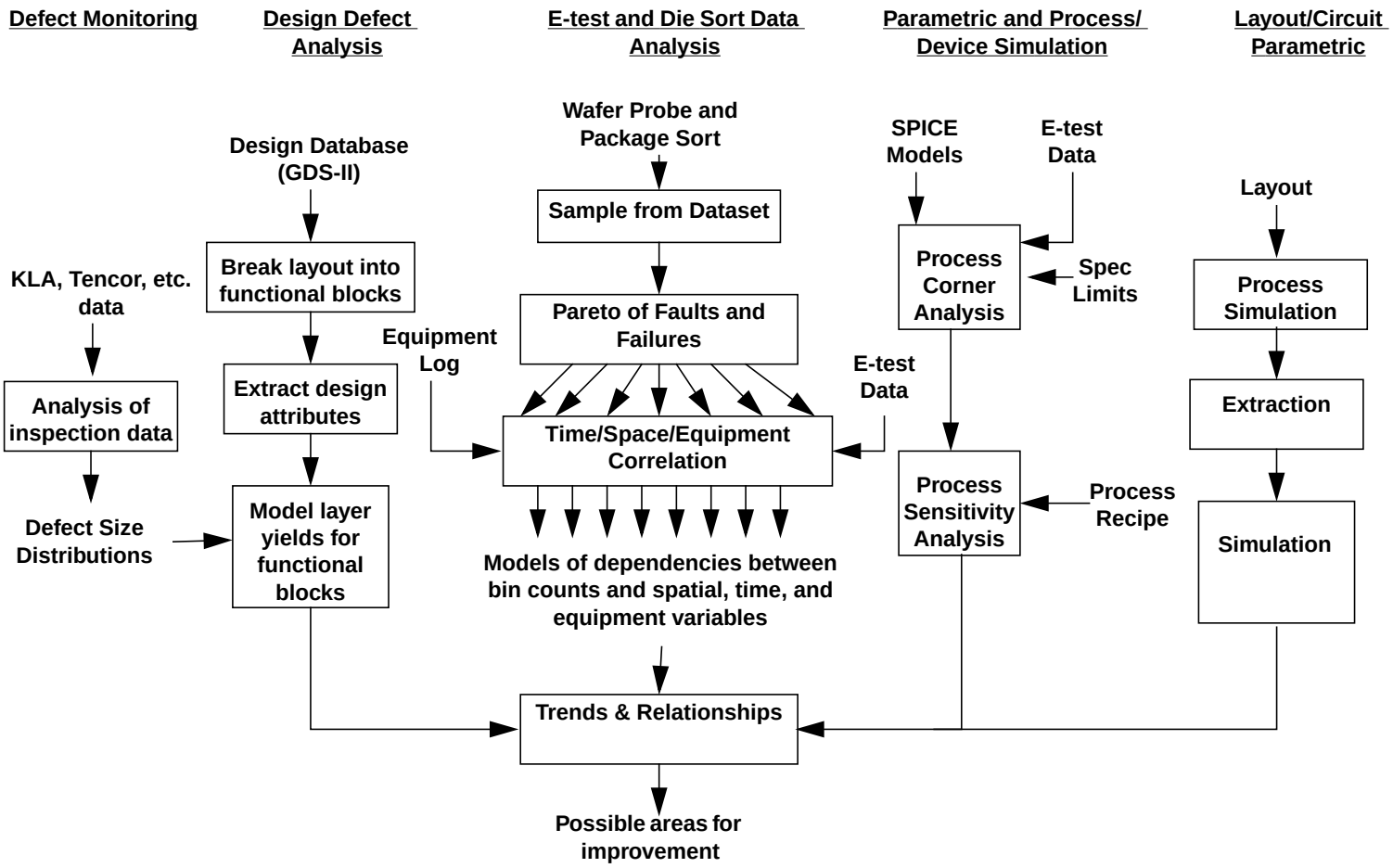

Figure 8. The components of holistic yield analysis.

failure signatures in memory probe-test bitmaps have been used extensively in the past for yield improvement. These data-driven efforts, however, have enjoyed comparatively little support from predictive yield models. In fact, “macro” yield predictions using the critical area of whole chips or large arrays are usually too coarse to provide insight into the physical mechanisms driving particular failure signatures. Consequently, significant quantities of in-line inspection and end-of-line test data must be gathered in order to determine empirical relationships between failure event signatures and physical failure mechanisms. In contrast, the key step in our methodology is a prediction of “micro-yield loss events” which directly correspond to the “failure event signatures” observed in bitmap and binmap test data. Examples of micro-yield loss events include individual logic block failures as well as memory array failures such as two, three or more adjacent row shorts; two three or more adjacent column shorts; row/

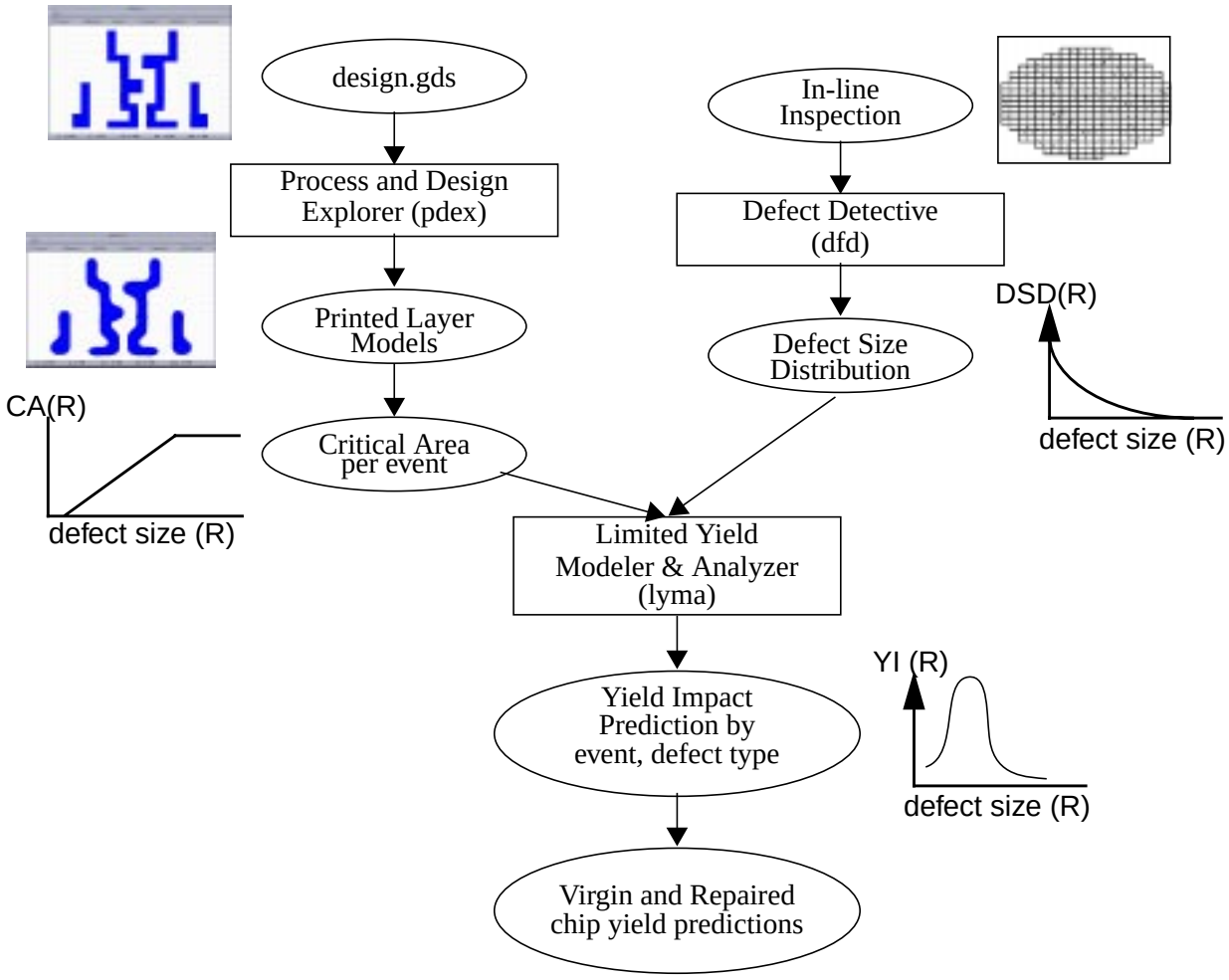

Figure 9. Defect limited yield prediction methodology.

column shorts and lack of contact to a cell. This “bottom up” prediction of failure events not only allows contrast-verification of probe test yields, but also provides an immediate correspondence between probe test results and individual failure mechanisms.

A detailed yield model has been developed for calculation of yield losses per failure mode per defect type. This yield model is formulated in terms of critical areas per defect type, and defect density and size distributions. For technologies with the design rules of 0.25μm and below, a layout printability simulation is performed first to obtain more realistic representation of the actual geometries on the wafer. Then critical areas leading to micro-yield loss events are computed using geometrical oversizing and categorizing resulting polygon overlaps according to the participating electrical nodes. Since each

critical area polygon is categorized into a single event class, all micro-yield predictions are guaranteed to be statistically independent. The style and extent of micro-yield loss events selected for modeling is determined by the redundancy scheme of a (possibly embedded) memory device and the resolution of the probe test results. Only those events which may be repairable must be modeled individually. In practice, however, it is often useful to model certain unrepairable failure events which are nonetheless observable in the probe test results and allow internal cross-validation of the yield models.

The next step in the methodology involves a chip-level yield prediction by combining a hierarchy of micro-yield loss events. Chip-, block- and cell-level repair constraints and resources, as well as unrepairable interactions between these levels determine the model hierarchy.

The final step of the methodology targets the absolute calibration of the yield models using in-line inspection data. Just as with the macro-yield predictions, micro-yield predictions require careful size-distribution analysis of in-line inspection data in order to accurately predict end-of-line yields. Data for such a calibration can be obtained from the early test chips that are being used for verification of cell designs (e.g., the cell array test chips with minimum peripheral circuitry). After the calibration step is performed, the resulting yield model can be used for derivation of optimal design rules, local optimization of array and periphery layouts, and evaluation of redundancy and error recovery/correction (ERC) needs. Moreover, defect targets per layer and type can be derived and transferred to the volume production fablines.

Another key component of our yield/performance ramp methodology is the employment of statistical device/process simulation (TCAD) to predict the distributions of electrical test values and SPICE parameters based on the distributions of equipment controls. This mapping of distributions can be performed in a number of ways. When the expected distributions are non-Gaussian (as they are for SPICE parameters which model complex effects such as subthreshold characteristics of a MOSFET), the most accurate way to accomplish this mapping is through Monte Carlo simulations.

The ability to use deterministic algorithms when extracting SPICE parameters is also a key part of the statistical characterization process. SPICE models are highly non-linear equations. The traditional way to

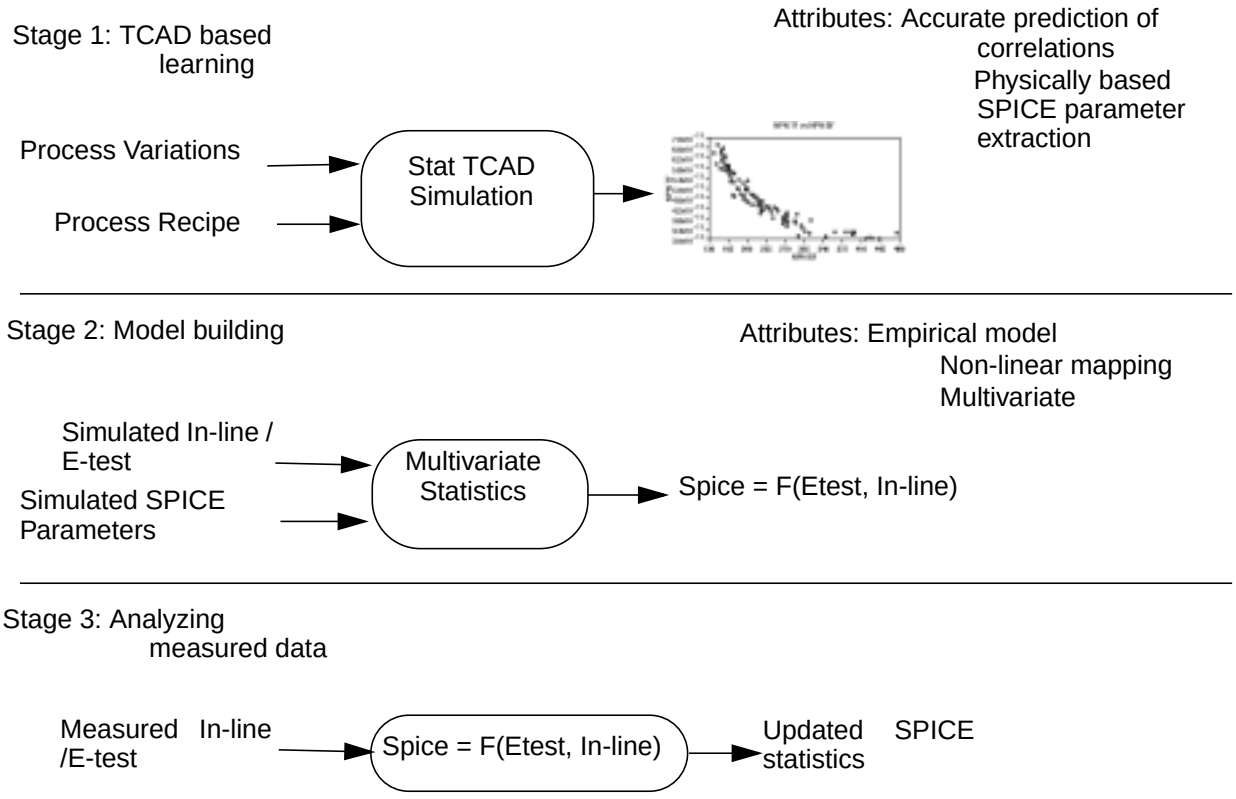

Figure 10. Approach to statistical characterization.

fit these equations is via gradient-based optimization. Since the objective function is complex, the solution is not unique, and hence not necessarily physical. The result is that while the fit is typically very good, if this procedure is applied to hundreds of devices to determine the effects of process perturbations on SPICE parameters, the obtained correlations tend to be difficult to interpret and are often not physical. It is shown that it is possible to use the information available from TCAD process simulations (such as actual dopant profiles) to extract the SPICE parameters in ways which cannot be typically accomplished from I-V characterization[11].

The last part of our statistical characterization process is to reduce a large distribution of SPICE parameters to an analytical model suitable for use inside commercial SPICE packages, which captures the variability of SPICE parameters due to both deterministic and random variations in the process. This is possible using advanced algorithms based on the principal component analysis (PCA), i.e., an eigenvalue/eigenvector decomposition of the correlation matrix. Principal component analysis allows us

to extract the underlying basic variables from the typically much larger number of correlated observables. Traditional PCA expresses SPICE parameters in terms of arbitrary random variables which have no physical meaning. For PCA-based algorithms to be useful for IC designers the software must interpret these factors and model the SPICE parameters in terms of E-tests.

PDF has implemented its holistic yield improvement methodology as part of its service offering to several large semiconductor companies. In all cases, the focus has been on leading edge deep submicron (<0.25um) technologies including microprocessors, logic and memory ICs. With this methodology, PDF has been able to consistently double the yield learning rate while achieving performance improvements of 10% to 20% over original specifications. This improvement in ramp rate can not be accomplished by traditional means. Only the additional insight and efficiency of leveraging simulations (where applicable) and the combined analysis of design, manufacturing and test data can provide the accelerated yield learning required by today's market.

IV. SUMMARY

A "holistic" yield improvement methodology has been proposed and implemented to significantly reduce the yield ramp time and maximize the profit for semiconductor manufacturer. This new approach to yield improvement bridges the gap between design and manufacturing by integrating process recipe and design information with in-line manufacturing data to gain an enhanced understanding and subsequent solution to solving the process and design architecture issues that affect yield and performance. With this methodology yield is improved not just by eliminating defects, but also by resolving parametric and systematic problems as well. The result is higher yield and performance in a fraction of the time required by traditional "defect based" methods. The more complex the product the better the pay back, making this approach especially useful in ramping yields of complex logic and system-on-a-chip products as well as DRAM and flash products.

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