Impact of Unrealistic Worst Case Modeling on the Performance of VLSI Circuits in Deep Sub-Micron CMOS Technologies

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Abstract— **The impact of process fluctuations on the variability of Deep Sub-Micron (DSM) VLSI circuits performances is investigated in this paper. In particular we show that, as process dimensions scale down in the sub half-micron region the relative weight of process variability tends to increase, thus wearing down a non negligible portion of the benefits that are expected from minimum feature size scaling. We will show that, in order to better exploit the advance of process technology, it is essential to adopt a realistic approach to worst case modeling, as the one described in [1] (APT). The application of the APT technique to different test circuits designed in 0.35μm, 0.25μm and 0.18μm CMOS technologies with a power supply ranging from 3.3V down to 1V will demonstrate how the manufacturability of DSM designs is going to be a vital factor for the successful implementation of high performance or low-power systems in 0.18μm and lesser technologies.**

Keywords— **Worst case model, Assigned Probability Technique, Performance spread, Process Fluctuations, Statistical design.**

I. Introduction

THE random variability of the parameters of the semiconductor fabrication process is reflected into a corresponding stochastic spread of the circuit performance [2]. In part this is due to the fact that the fabrication equipment, materials and control variables can not be controlled with infinite precision, but only within given tolerances. As their values drift and fluctuate over time, devices belonging to different wafers and lots are processed with slightly different physical and environment conditions. Another source of randomness is the imperfect spatial uniformity of the processing steps (for example gas flows, etching and deposition of materials, ion implantation, CMP etc.), which causes differences in the geometries and composition of the different patterned layers on the same chip and on the same wafer. The effect of equipment and material drift and fluctuations and of process non uniformity is to introduce spatial and temporal variations of the device parameters. These variations give rise to a hierarchy of random effects, such that a generic physical, electrical, or performance parameter of any particular device, circuit or system is best described as a stochastic process, $P(t, \vec{x})$ function of time (in other words of lot and wafer number) and of the spatial coordinates locating the device on the wafer surface. The effects of stochastic process variations have often been regarded as a problem affecting only full-custom, high-performance analog design. In fact, they have always been considered as a second order effect for VLSI digital designs, mainly because digital circuits offer a much superior noise rejection performance than analog circuits. However, as the design specifications and constraints rapidly tighten, less and less margin is left for circuit overdesign that is associated with unrealistic worst case modeling of circuit performances. This is going to be a serious concern, particularly for high-speed designs, like for example hi-end microprocessors, and also for low-power, low-voltage applications, e.g. portable devices such as cell phones, pagers and laptop computers, where high throughput has to be combined with extremely low levels of power consumption [2]. The simplest way of achieving these objectives is by concurrent scaling of the power supply and of the V_T of the devices [2], [3]. Unfortunately this solution will possibly decrease noise margin and thus further increase the relative importance of random fluctuations. It is thus obvious that a realistic way of modeling and characterizing intrinsic process randomness is becoming more and more important in order to design decently manufacturable electronic systems.

The most straightforward way of deriving worst case models of the behavior of electronic devices is to extract SPICE level model parameters corresponding to process corners (by using either corner lots, SPC or process and device simulations). In this way, the correlation among different device parameters is neglected, thus possibly originating worst case models that are extremely unlikely or even physically impossible.

Even if device correlations were taken into account, by addressing device level worst case performance, one neglects the circuit level correlation affecting the performance of basic building blocks, like standard cells or memory cells [4], [5], [6]. These correlations are introduced by the fact that VLSI library components are characterized by similar architecture, topology and sizing properties, hence their timing and power performance are likely to show very sim-

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ilar process sensitivity values.
This observation is the basis for alternative techniques [1], [7], [8], [9], [10] for more realistic worst case extraction. In particular, authors in [10] exploited the correlation between similar types of basic building blocks performance, in order to reduce the pessimism of worst-case simulation. The correlation was obtained from an empirical observation of the performance distribution resulting from SPICE model extraction and circuit simulations. The SPICE model parameters extraction was performed on routinely collected process fab electrical test data, and circuit primitives were grouped according to their experimentally observed correlation, allowing to identify one worst case model for each group of primitives. Similarly, authors in [1] proposed to use performance correlation measured from extensive Monte-Carlo simulations of cell library timing performance in order to identify clusters of percentile points corresponding to a pre-defined probability value. Response Surface Methodology (RSM) [11] was used in order to speed-up the Monte-Carlo runs and maximum likelihood in the process variable space was applied in order to identify a unique SPICE model for every cluster.
In this paper, we will first thoroughly examine the effects of random parameters variability on the manufacturability of some VLSI blocks (16 bit RC adder, Viterbi decoder) as a function of the concurrent scaling of technology and power supply value. We will then apply APT to derive realistic worst case models for the STMicroelectronics standard cell library designed in three different DSM CMOS technology generations (0.35μm, 0.25μm and 0.18μm). The standard cells have been designed with a full custum approach for maximum integration. We will then compare the performance predictions resulting from APT modeling with those obtained from usual worst case modeling techniques and with the results of the statistical simulations (Monte-Carlo) of the above mentioned circuits.
The objective is to demonstrate that:

i) the relative increase of the performance spread may become a critical issue for sub half-micron technologies for very low voltage since it seriously reduces the nominal advantage coming from a process shrink;
ii) a considerable amount of this performance loss may be recovered by simply considering a more realistic approach to worst case device modeling.

Even if interconnect contribution is becoming increasingly relevant to propagation delay, the effect of process variations is considered only on devices behavior since the scope of the analysis is to compare device-level to cell-level worst-case modeling methodologies.
The structure of this paper is as follows. In Section II we will examine the effect of process variability on some significant CMOS design blocks as a function of combined technology and voltage scaling. In Section III the application of a library-specific realistic worst case modeling technique to a set of DSM CMOS libraries will be illustrated. In Section IV we will compare the results obtained by different statistical modeling techniques on a set of test cases. Finally, in Section IV we will provide some conclusions.

II. Effect of technology and voltage scaling on process variability

As a practical example of the impact of technology and voltage scaling on the performance spread induced by process variability, we performed a set of Monte-Carlo circuit simulation on a 16-bit, ripple-carry adder implemented in three different CMOS technologies with minimum channel length 0.35μm, 0.25μm and 0.18μm. For each technology, the statistical behavior at the device level was described by a statistical MOSFET SPICE model based on a public domain MM9 model [12] in which only a reduced subset of parameters have been identified as independent stochastic variables. The subset of independent parameters is reported in Table I. In the simulation all transistor share the same model, and thus they are subject to the same parameter variations. The parameters experimental distributions are derived by pooling data coming from single-transistor measurements on several dies, so that the total parameter variability includes both within-die and between-die contributions. Mismatch between devices is not taken into account in order to limit the number of independent statistical variables. In this way, a trade-off between accuracy and computational complexity is achieved.

A Monte-Carlo analysis has been performed to derive the statistical distribution of the circuit performances from the device parameter statistics. The computational effort needed has been drastically reduced by using the Response Surface Method (RSM) to build second order polynomial models for the circuit performances, as described in [1]. In our case, a central composite design (CCD) [11] was used to generate the experimental design. The number of SPICE simulations required for each cell was thus 27 with 5 independent parameters (0.35μm and 0.25μm technologies) and 45 with 6 parameters (0.18μm technology). For all the polynomial models we achieved a goodness of fit R^2_{adj} always greater than 0.99. The nominal operating conditions for each of the three technologies are reported in Table II: V_{DD} is the supply voltage, TT is the input transition time and C_L is the capacitive load.

To determine the statistical behavior of the devices, electrical measurements were performed for stable processes such as 0.35μm and 0.25μm, while process device simulations were used for 0.18μm which was not mature yet. The device-level parameters were then extracted by using a mixed extraction-optimization based approach. A typical case model has been defined by setting all the parameters to their mean values. Combining the parameters corner values (3σ of the statistical distribution) achieving the worst/best device performance, a "classical worst-case" (CWC) SPICE model and a "classical best-case" SPICE model have been extracted for both n-channel and p-channel MOSFET in each of the three technologies.
With the help of RSM, the 16-bit adder critical path delay has been statistically evaluated, through a 20,000 sample Monte-Carlo analysis using second order polynomials.
The results of the Monte-Carlo analysis are summarized in Fig.1, which shows the Monte-Carlo-estimated probability density function of the critical path delay in each of the

three technologies. It is easy to see that, as the minimum feature size is reduced, the performance spread steadily increases. Furthermore, it should be noted that worst-case performance prediction based on the CWC model yields a fairly pessimistic result.

This is evident when the predicted worst case performance (stars in Fig.1) is compared to the percentile point corresponding to an assigned probability value (filled dots). Assuming a normal distribution for the timing performances (as it is in our case) a probability of 1.35×10^{-3} of a worse performance corresponds to $\mu+3\sigma$ of the distribution (called the 3σ percentile in the following).

Fig. 1. Statistical distribution of 16-bit adder critical path delay for 0.35μm (top), 0.25μm (middle), 0.18μm (bottom) technologies

Results are summarized in Table III, reporting the percent excess delay of the 3σ performance and that of the predicted worst-case performance with respect to the delay mean value for the three technologies at various supply voltages. As supply voltage is reduced, the margin between the 3σ performance and the worst-case model prediction dramatically increases. This trend becomes more evident with the reduction of the technology minimum feature size, to the point that the nominal advantage coming from technology scaling may be almost completely canceled by the overly pessimistic predictions of CWC-like models. This is shown in Fig.2(a), which reports the delays corresponding to the 3σ point (filled squares) and to the predictions of the worst-case model (filled diamonds), both normalized to the typical 0.35μm adder delay, as a function of minimum feature size. Fig.2(b) displays the same data normalized to the typical delay for each technology, so that the increase of the relative performance spread and of the margin between the 3σ point and the worst-case model prediction is evident.

Fig. 2. 16-bit adder critical path propagation delay normalized to the typical propagation delay of 0.35μm technology (a) and to the typical delay for each technology (b).

Fig. 3. Increase of the spread of 16-bit adder critical path propagation delay due to power supply scaling.

The same behavior is observed as power supply voltage is scaled down, as reported in Fig.3 for the 0.25μm adder. All data are normalized to the typical delay at the corresponding power supply voltage V_{DD}.

III. Realistic Worst Case Modeling

The results presented in the previous section clearly demonstrate that a circuit designed by using a classical approach to worst case modeling will make use of oversized devices because of the overly pessimistic prediction of circuit performance spread. In the following, we propose an alternative procedure, based on APT [1], to extract a unique, library-level, realistic worst case model. Since APT is performed on a selected subset of elementary standard cells at nominal power supply voltage, and it produces a unique model parameter set, the model prediction accuracy is then verified on a different set of cells, at multiple and different V_{DD} values. Finally we will use a synthesized IP block (Viterbi decoder) to test the APT accuracy prediction at the circuit and macro-block level.

The set of selected cells includes a static inverter, 2-input AND, NAND, OR, NOR and XOR gates, belonging to high-density standard cell libraries designed in the three DSM CMOS technology generations (0.35μm, 0.25μm and 0.18μm) described in the previous section. The timing behavior of each cell is described in terms of two or more different I/O delay paths. The statistical distribution of each I/O path delay is characterized by using an RSM-based Monte-Carlo analysis, following the same steps described in the previous section for the 16-bit adder critical path. The 3σ percentile of the probability density function of the k-th I/O path delay $t_k(3\sigma)$ is found, and the maximum likelihood set of model parameters $\vec{p}$ that minimizes the distance from the corresponding set of I/O path delays $\vec{t}_d(\vec{p})$ from the 3σ delay vector $\vec{t}_d(3\sigma)$ is obtained by using a numerical gradient search algorithm in the model parameter space S_M defined in Table I. The optimization problem has been formulated as follows:

$$\min_{\vec{p} \in S_M} = \left\{ \alpha \left[\sum_k \left(\frac{t_{d,k}(3\sigma) - t_{d,k}(\vec{p})}{3\sigma_k} \right)^2 \right] + \beta \left[\sum_i \left(\frac{p_i - \mu_i}{3\sigma_{p,i}} \right)^2 \right] \right\}$$

where μ_i is the mean value of the i-th parameter and α and β are weighting factors. For each library this procedure yields a unique model parameter set which we will refer to as the 3σ model. The ability of the 3σ-model to predict the worst-case performance at a corresponding level of probability for different cells is demonstrated in Fig.4, showing an histogram of the percent error between the performance predicted by the 3σ model extracted for the 0.25μm library at V_{DD}=2.5V and the 3σ performance estimated by Monte-Carlo analysis for various timing arcs. The maximum error is 3.56%.

The model extraction procedure can be repeated to extract the 3σ model in different operating conditions, for example, at different values of V_{DD}. At first order we may neglect the effect of the interaction between process and voltage variations. As a consequence, it is reasonable to expect that the 3σ model extracted at a given power supply voltage shall be able to predict with good accuracy the 3σ performances of the same library cells at different V_{DD} values. The absence of correlation between process and voltage variations allows to considerably reduce the computational effort required, as it is not necessary to repeat the worst-case extraction at different operating conditions. In order to validate this assumption we compared the Monte-Carlo performance estimations with the results of simulations performed by using the 3σ-model extracted at 2.5V and those obtained by using different 3σ-models re-extracted at each different V_{DD} value. This experiment

has been performed by varying the power supply over a V_{DD} range going from 1.3V to 2.8V.

Fig. 4. Distribution of the percentage error between the 3σ estimated by Monte-Carlo and the prediction of the 3σ model.

The results of this comparison are shown in Fig.5. The accuracy of the 3σ model extracted at V_{DD}=2.5V is good except at the lowest V_{DD} value considered (1.3V). This might be due to the fact that when the power supply voltage approaches the sum of the thresholds ($V_{TN}+|V_{TP}|$), the behavior of the CMOS cell is affected by both NMOS and PMOS device parameters. On the other hand, at higher V_{DD} values the timing properties of the cell for a given transition direction (rising or falling) is dominated by either the n-channel or the p-channel MOSFET device only. As a consequence, the original assumption that the effect of process and voltage variations can be considered to act independently on the cell performance does not hold any longer.

Fig. 5. Comparison between the 3σ performance estimations obtained by: Monte-Carlo analysis (circles), 3σ-model extracted at V_{DD}=2.5V(squares) and 3σ-model re-extracted at every different V_{DD} (triangles) for three different I/O paths delay 0.25μm.

Fig. 6. Monte-Carlo analysis on Viterbi critical path varying V_{DD}.

Up to this point we have analyzed the accuracy of the 3σ model for single cells only. On the other hand, the performance distribution of library cells should be strongly correlated to that of VLSI blocks based on that library, so that a library specific 3σ model should yield accurate predictions also at the block level. To verify this assumption, we compared the prediction of the 0.25μm library 3σ model, extracted at V_{DD}=2.5V, with the results of Monte-Carlo statistical characterization of the critical path of a Viterbi decoder. The RTL VHDL description of this block has been mapped on the 0.25μm library by using Design-Compiler [13]. The critical path topology was extracted by using DesignTime [13], a gate-level Static Timing Analyzer, and a corresponding spice level netlist has been obtained by properly setting the side inputs value. Both synthesis and critical path extraction were performed at nominal operating conditions, thus implicitly assuming that process and voltage variations do not affect the actual critical path topology but only its delay value. This assumption may not always hold true, because delay path sensitization may depend upon process variability under certain conditions, as discussed in [14]. The estimated distribution of the Viterbi decoder critical path at three different supply voltages (1.8, 2.5, 2.8V) is shown in Fig.6.

The 3σ percentile point of the Monte-Carlo distribution is compared with the prediction of the 3σ model, and with that of the classical worst-case model (CWC). It is possible to observe that the 3σ model still maintains a remarkable degree of accuracy even at macro-block level, whereas, as in the case of the 16-bit adder, the margin between CWC predictions and the actual 3σ performance percentile point is noticeable and it increases as V_{DD} is scaled down. This is more easily observed from the plots in Fig.7, in which the same data are shown as a function of power supply voltage V_{DD}. All data are normalized to the nominal delay value obtained at the corresponding power supply voltage. Again it is possible to observe that, not only the CWC methodology yields overly unrealistic predictions, but also this effect tends to further increase at lower V_{DD} values.

Fig. 7. Behavior of Viterbi critical path 3σ performance estimated by Monte-Carlo analysis (circles), predicted by the 3σ model (squares) and by CWC model (triangles).

IV. Conclusions

In this work, we have presented a detailed analysis of the effect of technology scaling on the statistical spread of the circuit performance for CMOS VLSI IC's. The analysis has been applied to circuits designed in advanced CMOS technologies, well below the sub-half micron region (from 0.35μm down to 0.18μm). It has been demonstrated that the variance of digital circuits timing performances tends to increase as device dimension and power supply are further scaled down, at the expenses of performance improvement margin. Furthermore, it has also been demonstrated that the predictions of performance spread by means of a traditional approach to worst-case modeling yields overly pessimistic results, thus severely reducing the benefits expected from technology scaling. In order to recover from this problem, we proposed to consider a different approach (APT), allowing to derive realistic worst case models for the timing analysis and simulation of VLSI circuits. This technique is based on the observation that a more realistic worst case model can be obtained by considering the correlation that is introduced by the fact that any synthesisable block will be eventually mapped on a common set of basic components (e.g. the standard cell library), and that a library specific worst-case model can be obtained by an RSM based statistical pre-characterization of the library. The results that we have obtained demonstrated an improvement in the predicted worst case performance up to 45% with respect to more standard worst case modeling strategies (CWC) when a 0.18μm, 1V power supply technology is considered. Furthermore, a positive trend of this improvement was shown as technology and power supply are scaled down.

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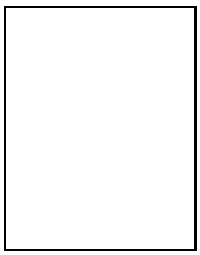

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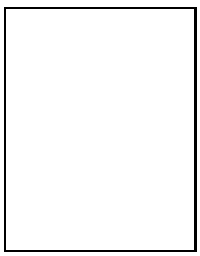

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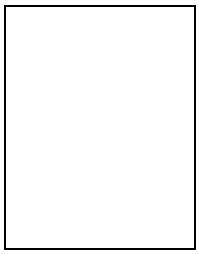

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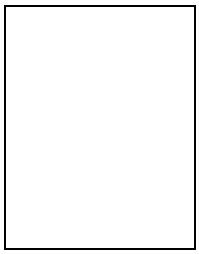

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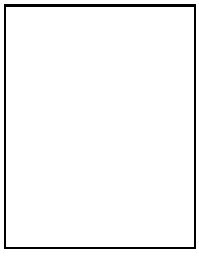

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TABLE I

THE INDEPENDENT SPICE PARAMETERS SETS FOR THE THREE TECHNOLOGIES.

Parameters	Description
tox	Thickness of the oxide layer
nvtor	Threshold voltage at zero back-bias for the nMOS transistor
pvtor	Threshold voltage at zero back-bias for the pMOS transistor
lvar	Difference between the programmed and the actual poly-silicon gate length
wvar	Difference between the actual and the programmed field-oxide opening
tpoly	Poly thickness (only used for 0.18μm technology)

TABLE II

OPERATIVE CONDITIONS FOR THE THREE TECHNOLOGIES.

	0.35μm	0.25μm	0.18μm
V_{DD}[V]	3.3	2.5	1.8
TT[ns]	0.2	0.05	0.04
C_L[pF]	0.082	0.063	0.051

TABLE III

PERCENT SPREAD FROM THE TYPICAL VALUE FOR THE 16-BIT ADDER CRITICAL PATH DELAY TIME.

V_{DD}[V]	3σ worst case model[%]	CWC model[%]	Margin gain[%]
0.35μm			
3.3	16.84	21.26	4.32
2.5	18.94	25.71	6.77
1.8	21.78	33.04	11.26
0.25μm			
2.5	21.41	29.06	7.65
1.8	26.54	38.95	12.41
0.18μm			
1.8	27.57	43.20	15.63
1.5	32.14	49.60	17.46
1.2	38.64	67.57	28.93
1.0	45.53	90.65	45.12