New methodology for ultra-fast detection and reduction of non-visual defects at the 90nm node and below using comprehensive e-test structure infrastructure and in-line DualBeam™ FIB

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Abstract

This paper describes a methodology to quickly capture, characterize, prioritize, localize, and perform in-line FA on killer defects. The system, which includes comprehensive short-flow test wafers, fast inline e-test, a powerful data analysis system, and advanced in-line dual beam inspection, was demonstrated in a leading-edge 300mm fab at the 90nm technology node to detect and resolve both systematic and random defect mechanisms greater than 10x faster than traditional methods. This article describes several examples of detecting and resolving non-visual (subsurface) as well as visual defects for both back-end and front-end issues.

Keywords

Failure Analysis, Non-visual Defects, Defect Localization, Advanced Metrology, Yield enhancement, Voltage Contrast.

INTRODUCTION

The need to accelerate the process of identifying, analyzing, prioritizing, and resolving electrical defects are becoming critical requirement of a successful product yield ramp at the 90nm node and below. This paper describes a comprehensive and proactive methodology to help capture, prioritize, analyze and resolve killer visual and non-visual defects faster than traditional methods.

Visual wafer inspections for particle-based defect mechanisms have enjoyed fast turn around time, since they can be detected visually, and the cycle of detection through process fix can often be completed without the need for complete full-flow processing. These visual particle or surface defects can often be detected on product wafers themselves, or on test chip wafers, with no need for any sophisticated electrical or defect analysis.

However, traditional methods to address non visual or buried defects rely on use of product wafers or SRAM test chips, combined with intensive visual inspection and off-line failure analysis. These approaches are limited because they are reactive, late in the manufacturing flow (require a SRAM functional test), and slow (require full flow processing). Additionally, the defects involved are often difficult to localize in a product, too sensitive to be captured by SRAM test structures, and require large number of wafers to obtain a statistically significant result in the 1-3 parts per billion (ppb) range that is required for achieving stable, yields in the 90nm node and below. Furthermore, the failure analysis is performed outside of the fab, which can take days to weeks. These issues strongly motivate a need for a fast methodology and framework to enable localization and failure analysis with greatly reduced turn around time and feedback.

A combined flow introduced by PDF Solutions and FEI Company was created to address these limitations. The flow provides a fast method for defect identification and reduction for modern technologies and has been proven at 90nm Cu for both FEOL and BEOL solutions.

METHODOLOGY

The new flow shown in Figure 1 below combines a suite of comprehensive short flow test chips, fast electrical test hardware designed specifically for testing the test chips, a powerful data analysis system, and an in-line DualBeam FIB, which has a focused ion beam and electron beam in the same system.

First, the process is characterized by processing test chip short-loop wafers containing specially designed, highly sensitive test structures (Characterization Vehicles® – CV's). These CV's are specifically targeted to capture electrical failures in back-end-of-line (BEOL) and front-end-of-line (FEOL) modules. The CVs contain a wide variety of structures that mimic process-design interactions that have been known, suspected, or hypothesized to cause yield losses in advanced nodes. Together, this group of test structures provides wide coverage across systematic and random defect mechanisms, down to 1-3 ppb failure range using a small number of wafers (~3-6 wafers). The CV short-loops are then rapidly electrically tested using a dedicated, massively parallel tester (pdFasTest™). The pdFasTest system is 10-15x faster than current parametric test systems, and can be set up inside the clean room environment, providing fast electrical test on the short-loop CV wafers.

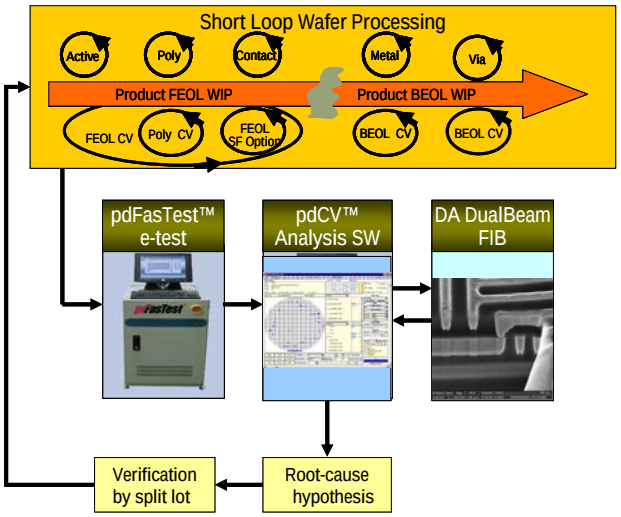

Figure 1. Methodology for rapid non-visual defect detection and failure analysis with wafer processing flow.

The test data is automatically sent to the pdCV™ analysis package, where the engineer or technician can perform detailed and accurate characterization of the process failure modes. The electrical test from the CV test chips are combined with any inline visual inspection data, to determine which electrical defects were also detected through traditional inline inspection methods. Based on this data, the user is able to select defects of particular interest for yield improvement, based on a wide variety of attributes.

After the electrical failures of interest have been selected in the pdCV analysis package, a file-based interface is utilized to send a file that can be read by FEI's Defect Analyzer (DA) 300 HP next-generation DualBeam™ system. This system uses a 2-pass method for localization and failure analysis. In the first pass, a technician or engineer manually identifies the failing location using voltage contrast techniques. In this work, open defects with >100M-ohm resistance and short defects <50K-ohms were localized. A fiducial marker is then milled at each location. About 30 sites per hour can be manually localized in this fashion. Defects of sizes down to 50-100nm can be localized in test structures as large as 40,000um^2. The second pass is an automated series of cross sectioning of all the localized defects. The DA system takes and records images during the cross sectioning process.

These images are then able to be loaded back into the pdCV analysis database, where they are linked to the particular electrical failures. Using these images, as well as the additional inline and electrical data stored in the database for these defects, the user is able to build image and defect Paretos to prioritize and drive yield improvement.

The following section describes results of the implementation of this methodology in a 300mm 90nm manufacturing facility.

RESULTS

The methodology described above was implemented in a 300mm wafer, volume manufacturing production facility running a 90nm manufacturing process. BEOL, Poly and FEOL CV test chips were deployed, together with the pdCV analysis software, pdFasTest system, and FEI DA300HP analysis station.

Back-end Module Results

The BEOL characterization used a 3 layer metal BEOL CV test chip from M1 through M3, including vias. The design of the CV included ~1000 product layout variations typically seen in SoC products. One example is via pitch. The test chip varies via pitch, via coverage, and impact of metal neighborhood of top and bottom metal. Another example is metal topography and impact on upper layer metal shorts. A full range of underlying metal density and upper metal spacings are designed in a rigorous DOE, so the impact can be statistically evaluated in the failure rate range required for advance nodes with a small sample of wafers.

The BEOL CV was run through the manufacturing line, and the typical in-line inspection was performed. The 300mm wafers were rapidly tested using pdFasTest tester, 3-4 hours per wafer, for all die and all structures. The resulting data was then loaded and processed in the pdCV software package.

Using the pdCV software system, the failure rates, yield, and failing locations can be determined for each structure type. The layout attributes can be evaluated and prioritized based on the failure rates, as well as the other inline data available. For example, M3 shorts due to underlying metal topography can be fully characterized to understand the densities, line widths, and line spaces that are sensitive to metal shorts.

In addition, electrical failures that did not receive corresponding inline defect hit can also be selected in the pdCV analysis software. In Figure 2 below, we show an example of selecting non-visual defects for a via chain with pitch > 2um with metal neighborhood. In the example, these via open failures with pitch 2.73um primarily impact the edge of the wafer. The selected failing test structures are chosen for failure analysis and exported to a file that can be read by the DA300HP DualBeam system.

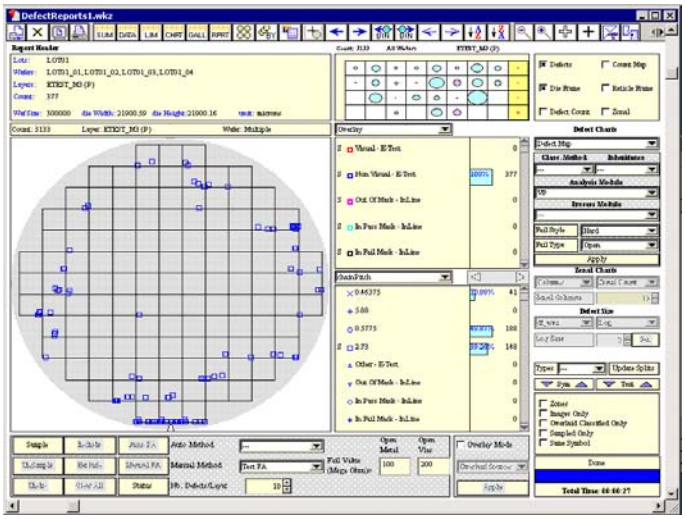

Figure 2. pdCV software interface for selection of electrical failures. In this example, vias with pitch of 2.73um which did not receive inline defect were chosen for FA.

Figure 3 illustrates the localization of a non visual defect in the long chain via structure. The exact location of the defect within the test structure is determined manually. Via opens identification using manual localization takes <2 min for a trained technician. After localization, the second pass then cross sections the defect using the FIB. The FIB and image capture can take as little as 7 min per site dependent on the image resolution and number of slices per defect. The results of this analysis are shown in Figure 4. The electrical failure is due to a metal voiding defect on the lower link of the chain.

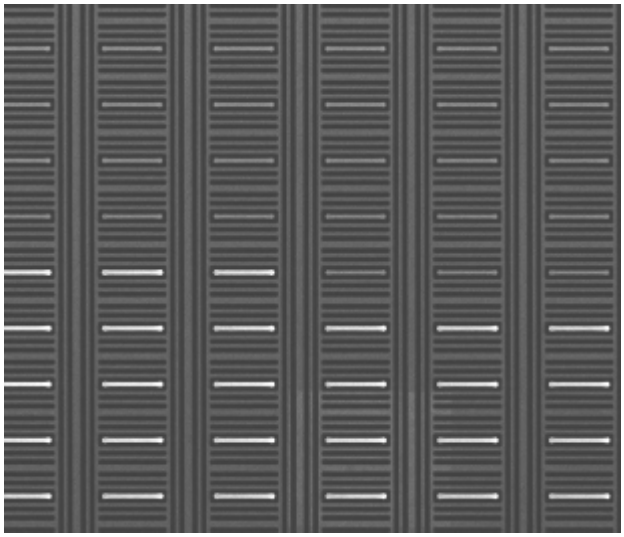

Figure 3. Top-down view of successful defect localization of a long chain via structure.

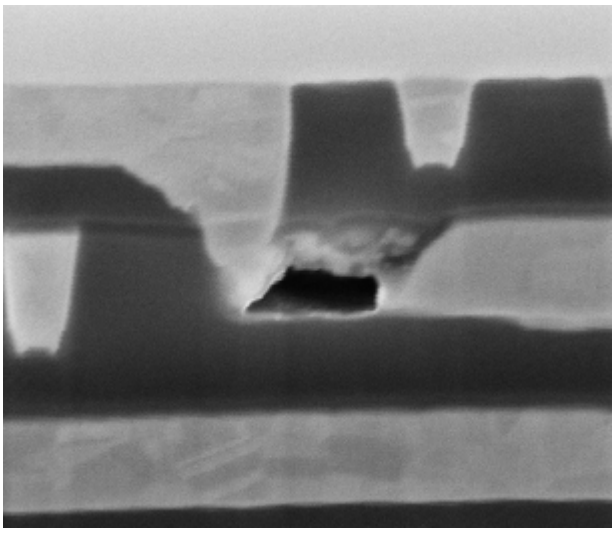

Figure 4. FIB cross section of large pitch via chain with via open failure.

Another example of a via open failure is shown in Figure 5. In this case, the the structure is a stacked M1 to M3 via chain. The image shows a void in the center of the bottom via, with the bottom interface of the via intact. This is a good example of a non-visual defect, as it can not be detected through inline optical inspection. However, it is easily and quickly identified and imaged using the methods presented here.

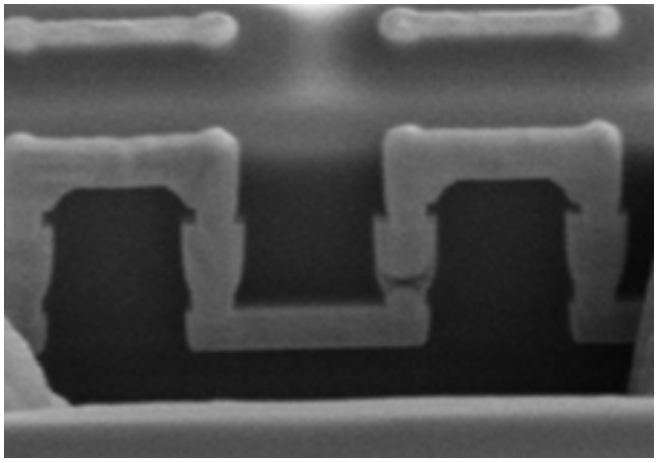

Figure 5. Dense via chain open. Lower level via has metal void causing structure to fail.

Metal opens and shorts are also supported with this methodology. Metal opens are localized quickly (<2 min per site) while metal shorts takes slightly longer, but generally is less than 15 minutes per defect failure. Figure 6 shows a metal short that was isolated using the FIB and voltage contrast techniques.

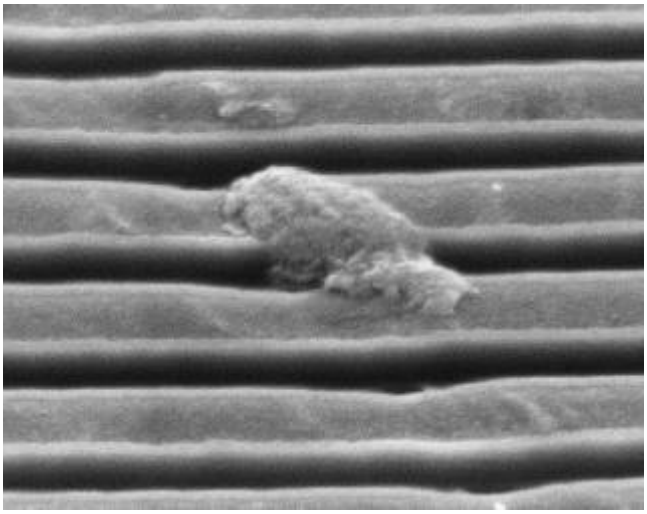

Figure 6. A shorting defect isolated in a failing structure. This defect can now be cross sectioned and material analysis can be performed immediately.

Poly Module Results

The next example was detected using the POLY CV test chip. This test chip characterizes the STI, poly, and silicide modules. Poly structures over both field and active with varying designed experiments are included, and the test chip can be used for both functional and parametric characterization.

Figure 7 illustrates a top-down image of a poly short defect. In this case, the test structure of interest is a poly snake and comb structure, with underlying active topography. The resulting defect can then be cross sectioned using the FIB milling techniques described above to aid in root cause determination.

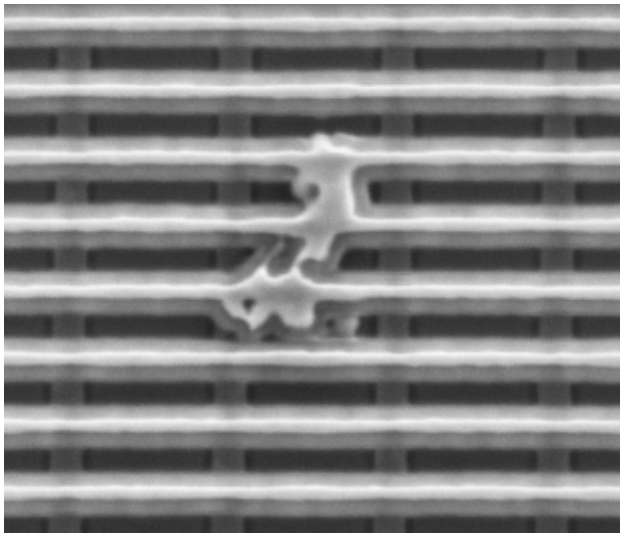

Figure 7. A poly short defect isolated within a failing structure.

Contact Module Results

Another failure mode explored included contact opens. The FEOL CV performs extensive characterization of contacts, and in this process technology, the contacts were metal contacts to local interconnect. Figure 8 shows a FIB cross section of a contact to local interconnect open. A foreign residue layer is suspected to cause the electrical open of the contact. Isolation of the defect using voltage contrast techniques assures us that this is an electrical open defect.

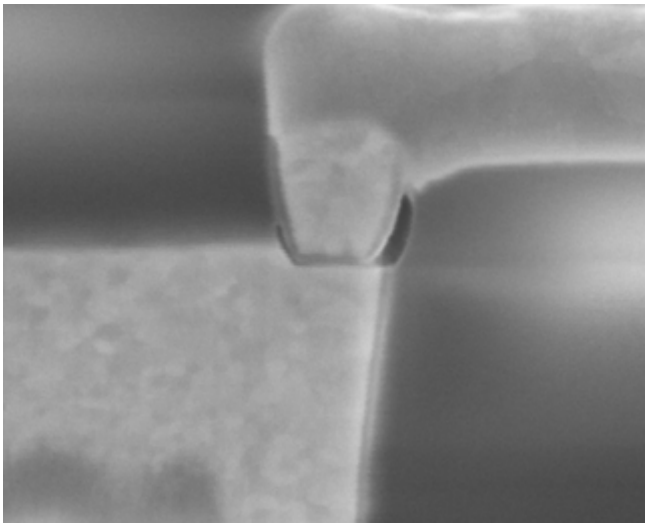

Figure 8. Contact to local interconnect defect found after FIB cross section was performed.

CONCLUSIONS

An integrated methodology was developed for rapid localization and failure analysis of failing electrical test structures, providing a framework for the rapid localization and failure analysis of both non-visual and visual defects. The methodology utilizes short flow CV test chips, to provide accurate failure detection and facilitate fast learning cycles. The CVs are tested on the PDF pdFasTest parallel tester, and the data is loaded in the pdCV analysis software system. The DA300HP DualBeam FIB system interfaces with the pdCV analysis package, providing powerful localization and analysis capability. Finally, the system was demonstrated to be successful at multiple process layers in the front-end and back-end modules in a 300mm wafer production facility currently manufacturing at the 90nm node.

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